Curriculum Vitae of Dr. Nalesh S

1. Name : Dr. Nalesh S

2. Address : Sivanandavilasom, Nedumon PO, Adoor, Pathanamthitta Dist. , Kerala - 691556.

3. Date of Birth : 15-05-1982

4. Academic Qualifications:

Degree	University	Year of passing	Subjects/ Specialization	Class
B. Tech.	National Institute of Technology, Calicut	2003	Electronics & Communication	1st Class with Distinction
M. Tech	Indian Institute of Technology, Delhi	2010	Integrated Electronics & Circuits	First Rank GPA 9.63/10
Ph.D	Indian Institute of Science, Bangalore	2018	High Performance Reconfigurable Architecture	GPA 7.6/8

5. Organizational Positions Held

- IEEE Member since 2013

6. Professional Experience:

Designation	Institution	Period
Systems Engineer	Wipro Technologies Bangalore	Sep 2003 – May 2008
Teaching Assistant	IIT Delhi	Aug 2008 - May 2010
ASIC Engineer	Brocade Communications, Bangalore	June 2010 – July 2012
Assistant Professor	Department of Electronics, Cochin University of Science and Technology	March 2018 – till date

7. Scholarships

- GATE Scholarship during MTech - IIT Delhi
- MHRD Scholarship for pursuing PhD – IISc Bangalore

8. Fields of Research and Teaching:

VLSI Design, FPGA Based System Design, Digital System Design and Verification, Reconfigurable Architectures, DSP Architectures, Machine Learning

9. Projects Undertaken:

10. Professional Training Experience:

11. Conferences & Workshops Attended:

- IEEE International Symposium on Circuits And Systems (ISCAS) 2013 at Beijing , China
- Embedded Systems Week (ESWEEK) 2014 at New Delhi, India
- IEEE International Symposium on Nanoelectronic and Information Systems(iNIS) 2015 at Indore, India
- 2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2015 at Austin, Texas, USA

12. Books Edited:

S. Kala, **S. Nalesh**, Babita R. Jose and Jimson Mathew, "Image Reconstruction Using Novel Two-Dimensional Fourier Transform", Book Chapter in Advances in Soft Computing and Machine Learning in Image Processing, Springer 2018, ISBN: 978-3-319-63754-2

13. Technical Reports Brought Out:

14. Symposiums Organized:

15. Number of Students registered for Ph.D ***(Guide)*** **: 0**
(Co-Guide) **: 0**

16. Projects Guided:
M.Tech/ M.Sc **: 0**

17. Invited Talks Delivered

1. Tutorial Speaker at *Embedded Systems Week* Oct 12-17, 2014 at New Delhi India, organized by Prof. S K Nandy , CADLab, IISc, Bangalore and Dr. Ranjani Narayan, CEO, Morphing Machines Bangalore.
   Topic: Run-time Reconfigurable High Performance SoCs,

18. Patents Filed

19. Awards

- Qualified GATE in 2003, 2004, 2005 and 2008.
  All India Rank (EC) 86 in 2008
- **Wipro Feather-in-my-cap Award** in recognition of fast ramp-up to handle multiple projects, providing customer support and getting involved in customer critical activities, in Aug 2004
- **Wipro Thanks-a-Zillion Award** in recognition of support for FUSIV-SPORT activity in getting the test setup running and providing hardware support, in June 2005
- **Wipro Feather-in-my-cap Award** in recognition of delivering H264 decoder test set-up and diagnostics of FPGA platform with stringent deadlines, in Nov 2006

List of Publications

International Conferences

1. Kala S., **S. Nalesh,** Babita R. Jose, Jimson Mathew, Marco Ottawi,Two dimensional FFT architecture based on Radix-4^3 algorithm with efficient output reordering, in *13th IEEE Design and Technology of Integrated Systems in Nanoscale Era (DTIS)* 2018, Taormina, Italy, April 10-12, 2018
2. S. Das, **S. Nalesh**, K. T. Madhu, S. K. Nandy, and R. Narayan, RHyMe: REDEFINE HyperCell multicore for accelerating HPC kernels, in *29th International Conference on VLSI Design and 15th International Conference on Embedded Systems, VLSID 2016*, Kolkata, India, January 4-8, 2016, pp. 601602, 2016
3. **S. Nalesh**, K. T. Madhu, S. Das, S. K. Nandy, and R. Narayan. Energy aware synthesis of application kernels expressed in functional languages on a coarse grained composable reconfigurable array. In *2015 IEEE International Symposium on Nanoelectronic and Information Systems*, pages 7-12, Dec 2015
4. K. T. Madhu, S. Das, **S. Nalesh**, S. K. Nandy, and R. Narayan, Compiling HPC kernels for the REDEFINE CGRA, in 17th *IEEE International Conference on High Performance Computing and Communications, HPCC 2015*, New York, NY, USA, August 24-26, 2015, pp. 405410, 2015
5. F. Merchant, Arka Maity, Mahesh Mahadurkar, Kapil Vatwani, Ishan Munje, Madhava Krishna, **S. Nalesh**, Nandhini Gopalan, Soumyendu Raha, S.K. Nandy, Ranjani Narayan, Micro-architectural Enhancements in Distributed Memory CGRAs for LU and QR Factorizations, *2015 28th International Conference on VLSI Design*, VLSID, Bangalore, 2015, pp. 153-158
6. Ipsita B Mahapatra, Santhi N, **S. Nalesh**, S. K Nandy, SIMAAH:RTL simulation accelerator for complex SoCs, *IEEE International Conference on Electronics, Computing and Communication Technolgies (CONECCT)*, IISc Bangalore, 2015
7. S. Kala, **S. Nalesh**, S. K. Nandy and R. Narayan, Energy Efficient, Scalable, and Dynamically Reconfigurable FFT Architecture for OFDM Systems, *2014 Fifth IEEE International Symposium on Electronic System Design (ISED)*, Surathkal, 2014, pp. 20-24.
8. K. T. Madhu, S. Das, M. K. C, **S. Nalesh**, S. K. Nandy, and R. Narayan, Synthesis ofinstruction extensions on HyperCell, a recongurable datapath, in *XIVth International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, SAMOS 2014*, Agios Konstantinos, Samos, Greece, July 14-17, 2014, pp. 215224, 2014
9. S. Kala, **S. Nalesh**, S. K. Nandy and R. Narayan, Design of a low power 64 point FFT architecture for WLAN applications, *2013 25th IEEE International Conference on Microelectronics (ICM)*, Beirut, Lebanon, 2013, pp.1-4.
10. S. Kala, **S. Nalesh**, A. Maity, S. K. Nandy and R. Narayan, High throughput, low latency, memory optimized 64K point FFT architecture using novel radix-4 butterfly unit, *2013 IEEE International Symposium on Circuits and Systems (ISCAS 2013)*, Beijing, 2013, pp. 3034-3037.

Journals

International

1. M. Mohammadi, A. Krishna, **Nalesh. S**. and S. K. Nandy, "A Hardware Architecture for Radial Basis Function Neural Network Classifier," in *IEEE Transactions on Parallel and Distributed Systems*, vol. PP, no. 99, pp. 1-1.
2. **Nalesh S**., Kavitha T. Madhu, Saptarsi Das, S.K. Nandy, Ranjani Narayan, Energy aware synthesis of application kernels through composition of data-paths on a CGRA, *Integration, the VLSI Journal*, Available online 28 February 2017, ISSN 0167-9260, https://doi.org/10.1016/j.vlsi.2017.02.009.
3. S. Kala, **S. Nalesh**, S. Nandy, and R. Narayan, Scalable and Energy Efficient, Dynamically Reconfigurable Fast Fourier Transform Architecture, *Journal of Low Power Electronics*, vol. 11 (3): 426-435 *(*2015*)*
4. S. Das, K. T. Madhu, M. Krishna, **S. Nalesh**, F. Merchant, S. Natarajan, I. Biswas, A. Pulli, S. K. Nandy, and R. Narayan, A framework for post-silicon realization of arbitrary instruction extensions on recongurable data-paths, *Journal of Systems Architecture - Embedded Systems Design*, vol. 60, no. 7, pp. 592614, 2014.

Workshops

1. S. Das, **S. Nalesh**, K. T. Madhu, S. K. Nandy, and R. Narayan, Accelerating hpc kernels with RHyMe-REDEFINE HyperCell multicore, in *2016 MULTI-PROG Workshop*, Co-located with HiPEAC 2016, Prague, Czech Republic, 2016.
2. Madhava Krishna, **Nalesh S**, Kavitha Madhu, Saptarsi Das, Chandan Haldar, S. K. Nandy, Ranjani Narayan**,** Combating Dark Silicon in Polymorphic Massively Parallel Processing Cores, Dark Silicon Workshop at 2*015 IEEE/ACM International Conference on Computer-Aided Design ICCAD 2015*, Austin,TX
3. **Nalesh S**, Kavitha Madhu, Saptarsi Das, S. K. Nandy, Ranjani Narayan, Composition of Data-paths on a CGRA for Energy Aware Synthesis of Functionally Specified Application Kernels Dark Silicon Workshop at *2015 IEEE/ACM International Conference on Computer-Aided Design ICCAD 2015*, Austin,TX