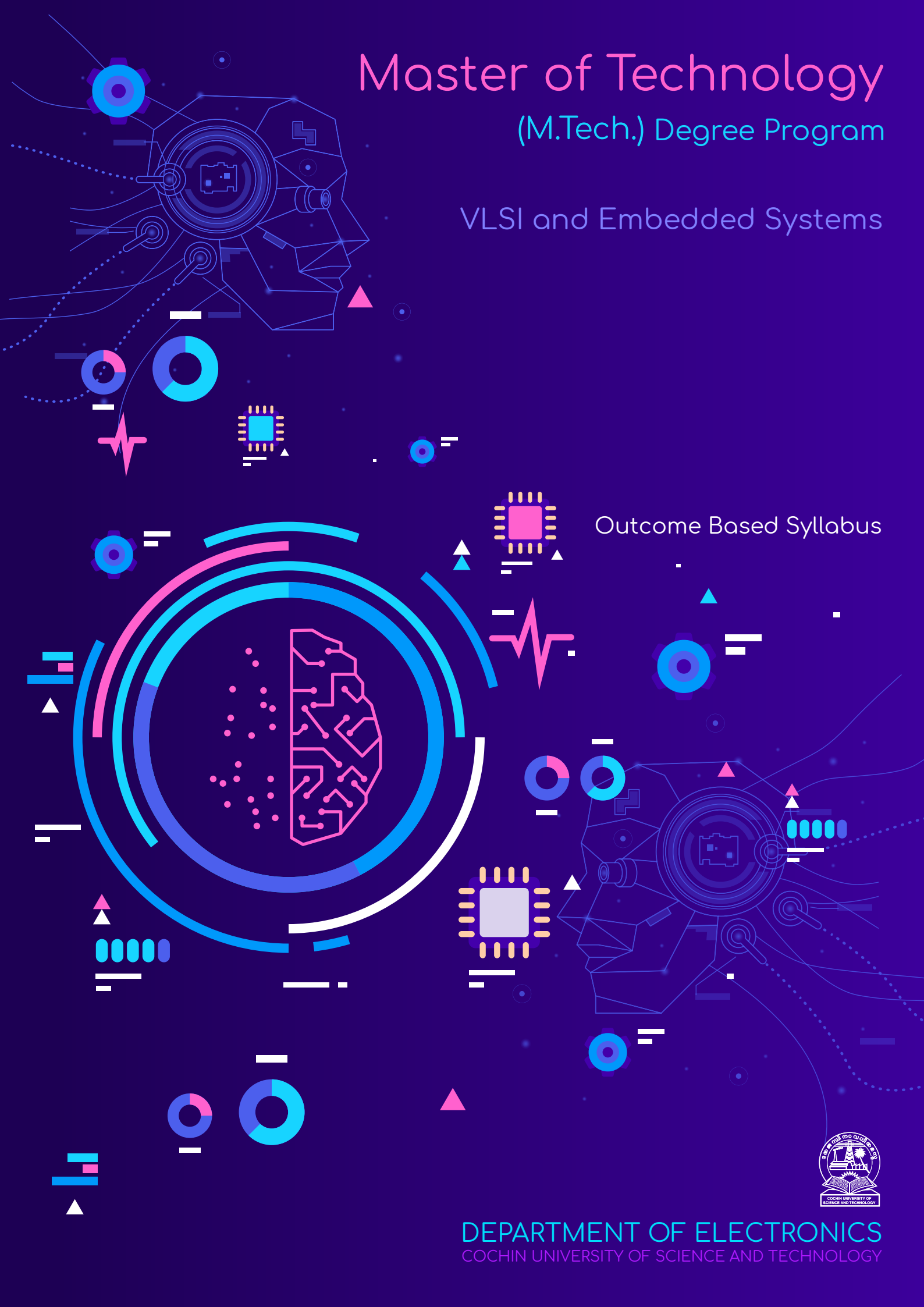
Master of Technology

(M.Tech.) Degree Program

VLSI and Embedded Systems

Outcome Based Syllabus



DEPARTMENT OF ELECTRONICS
COCHIN UNIVERSITY OF SCIENCE AND TECHNOLOGY

MASTER OF TECHNOLOGY

in

VLSI AND EMBEDDED SYSTEMS

Syllabus

(2025 Admission Onwards)

DEPARTMENT OF ELECTRONICS

COCHIN UNIVERSITY OF SCIENCE AND TECHNOLOGY

Kochi - 682 022, India

Contents

DEPARTMENT OF ELECTRONICS

VISION

To nourish and tone the legendary status in the field of Electronics by inspiring knowledge seekers to meet the challenges of evolving technology through innovative practices

MISSION

M1 : *To strengthen technical education in Electronics for graduates by utilising the state of the art facilities and adopting latest trends in technology*

M2 : *To impart knowledge and skills so as to kindle innovation & creativity among students leading to a progressive global career in industry & academy*

M3 : *To facilitate best opportunities for challenging young minds fostered through interaction with leading research organizations as well as industry*

M4 : *To develop and sustain a culture of focused work based on societal needs*

M5 : *To provide with avenues for recognition by participation in challenging platforms, while upholding values, ethics and professionalism*

PROGRAM EDUCATIONAL OBJECTIVES

Graduates will have

PEO1	Graduates apply their technical competence in theory, hardware, software and EDA tools to solve engineering problems in their chosen specialization
PEO2	Graduates apply their communication skill, leadership quality, research aptitude and ethics to build a strong career in their chosen areas of specialization through continuous learning
PEO3	Graduates develop capabilities for occupying prominent professional positions in academia, industry, research, and entrepreneurship

PEO-Mission Matrix:

Mission	PEO1	PEO2	PEO3
M1	✓	✓	
M2		✓	✓
M3	✓		✓
M4	✓		✓
M5	✓		✓

Programme Outcomes: At the end of the programme, the student will be able to

PO1	Apply engineering knowledge to carry out research, and analysis of technical problems
PO2	Develop solutions and design system components or processes that meet the specified needs considering all constraints
PO3	Create, select, and apply appropriate techniques, resources, and modern engineering tools
PO4	Ability to communicate effectively by preparing and presenting technical reports
PO5	Apply professional ethics and responsibilities in engineering practice
PO6	Engage in lifelong learning independently to enhance knowledge and skills that can contribute to the continuous improvement of individuals and society

Programme Specific Outcomes: At the end of the programme, the student will be able to

PSO1	Acquire competency in design, testing, verification and prototype development focusing on applications in areas of VLSI and Embedded Systems
PSO2	Integrate subsytems to develop embedded/intelligent/integrated circuit systems to solve real life problems
PSO3	Proficiency in using off the self electronic design and automation tools to develop systems for a given application

PEO-PO/PSO Mapping:

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
PEO1	✓	✓	✓				✓	✓	✓
PEO2				✓	✓	✓			
PEO3	✓	✓	✓	✓	✓	✓	✓	✓	✓

COURSE STRUCTURE

Semester 1

No.	Course Code	Course Title	L	T	P	Credits	C/E	CA	ES	Total
1	25-509-0101	Digital System Design using HDLs	3	2	0	3	C	50	50	100
2	25-509-0102	Digital Integrated Circuits	3	2	0	3	C	50	50	100
3	25-509-0103	Advanced Embedded System Design	3	2	0	3	C	50	50	100
4	25-509-0104	Digital System Design using HDLs Lab	0	0	4	2	C	100	0	100
5	25-509-0105	Digital Integrated Circuits Lab	0	0	4	2	C	100	0	100
6	25-509-0106	Intelligent Embedded Systems Lab	0	0	4	2	C	100	0	100
7	25-509-01XX	Program Elective	3	1	0	3	E	50	50	100
8	25-509-01XX	Program Elective	3	1	0	3	E	50	50	100
		Interdepartmental Elective*				3	E	50	50	100
Total						21				

Semester 2

No.	Course Code	Course Title	L	T	P	Credits	C/E	CA	ES	Total
1	25-509-0201	Design Verification and Testing	3	2	0	3	C	50	50	100
2	25-509-0202	FPGA Based Embedded SoC Design	3	2	0	3	C	50	50	100
3	25-509-0203	Design Verification and Testing Lab	0	0	4	2	C	100	0	100
4	25-509-02XX	Program Elective	3	1	0	3	E	50	50	100
5	25-509-02XX	Program Elective	3	1	0	3	E	50	50	100
6	25-509-02XX	Program Elective	3	1	0	3	E	50	50	100
		Interdepartmental Elective*				3	E	50	50	100
7	25-509-02XX	Program Elective Lab	0	0	4	2	E	100	0	100
Total						19				

* At least one interdepartmental elective is mandatory. Need to compulsorily register for the same before third semester. This can be opted instead of a program elective in either first or second semester.

Semester 3

No.	Course Code	Course Title	L	T	P	Credits	C/E	CA	ES	Total
1	25-509-0301	Project : Part 1	0	0	28	14	C	100	100	200
2	25-509-0302	Elective: MOOC/NPTEL Course#				2	E	0	100	100
		Total				16				

At least one MOOC/NPTEL course is mandatory. Need to compulsorily register for the same before registering for fourth semester exam.

Semester 4

No.	Course Code	Course Title	L	T	P	Credits	C/E	CA	ES	Total
1	25-509-0401	Project : Part 2	0	0	32	16	C	100	100	200
		Total				16				

Electives

No.	Course Code	Course Title	L	T	P	Credits	C/E	CA	ES	Total
1	25-509-0X11	VLSI Technology	3	1	0	3	E	50	50	100
2	25-509-0X12	VLSI Design Automation	3	1	0	3	E	50	50	100
3	25-509-0X13	Low Power VLSI	3	1	0	3	E	50	50	100
4	25-509-0X14	Neural Networks	3	1	0	3	E	50	50	100
5	25-509-0X15	Analog & RF IC Design	3	1	0	3	E	50	50	100
6	25-509-0X16	Robotics Technology	3	1	0	3	E	50	50	100
7	25-509-0X17	Device Physics and Modeling for Integrated Circuits	3	1	0	3	E	50	50	100
8	25-509-0X18	Advanced Computer Architectures	3	1	0	3	E	50	50	100
9	25-509-0X19	Deep Neural Network Signal Processing	3	1	0	3	E	50	50	100
10	25-509-0X20	Image & Video Processing	3	1	0	3	E	50	50	100
11	25-509-0X21	Advanced Digital Signal Processing	3	1	0	3	E	50	50	100
12	25-509-0X22	Real Time Operating Systems	3	1	0	3	E	50	50	100
13	25-509-0X23	Image & Video Processing Lab	0	0	4	2	E	100	0	100
14	25-509-0X24	Robotics Lab	0	0	4	2	E	100	0	100
15	25-509-0X25	Semiconductor Device Modeling Lab	0	0	4	2	E	100	0	100
16	25-509-0X26	Processor Architecture Lab	0	0	4	2	E	100	0	100
17	25-509-0X27	Deep Neural Network Signal Processing Lab	0	0	4	2	E	100	0	100
18	25-509-0X28	FPGA System Design Lab	0	0	4	2	E	100	0	100

19	25-509-0X29	Analog IC Design Lab	0	0	4	2	E	100	0	100
20	25-509-0X30	Neural Networks Lab	0	0	4	2	E	100	0	100
21	25-509-0X31	Real Time Operating Systems Lab	0	0	4	2	E	100	0	100

MASTER OF TECHNOLOGY

in

VLSI & EMBEDDED SYSTEMS

Semester 1

DEPARTMENT OF ELECTRONICS

COCHIN UNIVERSITY OF SCIENCE AND TECHNOLOGY

Kochi - 682 022, India

25-509-0101 **Digital System Design Using HDLs**

L	T	P	C
3	2	0	3

Prerequisites : Digital design
Course Description : This course trains the students to design digital system using HDLs and provides an overview of building a processor using basic components.
Course Outcome : After the completion of the course, student will be able to

CO1	Design combinational and sequential circuits	Apply
CO2	Design basic combinational/sequential building blocks of a digital system using Verilog/Bluespec HDLs	Apply
CO3	Compare different implementations in terms of timing and hardware resources	Analyze
CO4	Understand RISC processor pipeline and design a simple processor that support a subset of instruction	Apply

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	2					3	2	
CO2	3	3	3	2			3	3	3
CO3	3	3	3				3	3	3
CO4	3	3					3	3	3

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Review of Digital Design:** Combinational Logic - Karnaugh Maps, Sequential Circuits- Flip Flops and Latches, Mealy and Moore Circuits, State Reduction, Sequential Circuit Timing
Module 2	**Verilog HDL:** 4-Valued Logic System, Compilation, Simulations and Synthesis, Basic Constructs- Modules, Variables, Data types and Operators, Delays, Constants, Assignments, Initial and Always block, Blocking and Nonblocking Assignments, Statements – if, case, and casez, Constants arrays and loops, Structural model and Behavioral models, Testbench
Module 3	**Digital Building Blocks:** decoder, multiplexers, code converters, counters, shift registers, FSMs, Arithmetic Circuits -adders, multipliers, dividers, Number Systems (fixed and floating point), Sequential Building Blocks, Memory Arrays, Logic Arrays

Module 4	**Bluespec Verilog (BSV) HDL:** BSV's advantages over Verilog, Basic Syntax, Combinational Structures: Types and Type-checking, Parameterized Description, Sequential Design: Registers, Methods and method types, Rules and atomicity, Guarded interfaces, Iterative circuits: spatial and temporal unfolding, BSV to RTL: Interface, Registers, Ready-Enable interface protocol; Linearizability and Serializability, Concurrent execution of rules, rule scheduler
Module 5	**Processor Design:** MIPS ISA, Microarchitecture - Performance Analysis, Pipelined Processor- Data path, Control Path, HDL Representation-Instruction Encoding, Implementation of MIPS Subset

References:

[1] Charles H. Roth Jr., Lizy Kurian John, and Beyeong Kil Lee, *Digital Systems Design Using Verilog.* CL Engineering, 2015.

[2] David Money Harris and Sarah L Harris, *Digital Design and Computer Architecture.* Elsevier, 2019.

[3] Charles H. Roth Jr, *Fundamentals of Logic Design.* CL Engineering, 2013.

[4] Arvind, Rishiyur S. Nikhil, James C. Hoe, and Silvina Hanono Wachman, "Introduction to digital design as cooperating sequential machines."

[5] Bluespec Reference Guide, "https://web.ece.ucsb.edu/its/bluespec/doc/BSV/reference-guide.pdf."

[6] Rishiyur S. Nikhil and Kathy R. Czeck, *BSV by Example: The next-generation language for Electronic System Design,.* Bluespec, 2010.

[7] Stuart Sutherland, Simon Davidmann, and Peter Flake, *SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling.* Springer, 2006.

[8] John F. Wakerley, *Digital Design Principles and Practice.* Pearson Education, 2018.

[9] Samir Palnitkar, *Verilog HDL.* Pearson Education, 2004.

[10] J. Bhasker, *A Verilog HDL Primer.* Star Galaxy Publishing, 2005.

25-509-0102 **Digital Integrated Circuits**

L	T	P	C
3	2	0	3

Prerequisites : MOSFET basics, digital design
Course Description : This course introduces students to the analysis and design of digital integrated circuits along with the trade-offs involved in the design of combinational and sequential circuits.
Course Outcome : After the completion of the course, student will be able to

CO1	Apply MOSFET characteristic equations to understand the design trade-offs in static CMOS inverters	Apply
CO2	Implement a combinational logic circuit for a given functionality with specific speed, area and power requirements	Apply
CO3	Analyze functionality, area, performance and power dissipation of combinational and sequential circuits	Analyze
CO4	Illustrate the use of combinational and sequential circuit design principles for building efficient arithmetic circuits	Apply
CO5	Summarize the different implementation strategies for digital circuits and the impact of interconnects on these circuits	Understand

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	2					3		
CO2	3	3					3		
CO3	3	3					3	2	
CO4	3	3					3	2	
CO5	3						3		

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Introduction:** Issues in digital integrated circuit design, quality metrics, manufacturing process, static & dynamic behavior of MOSFETs, interconnects **Static CMOS Inverter:** CMOS inverter, static & dynamic behavior, robustness, performance, sizing, power dissipation
Module 2	**Combinational Logic:** Complementary CMOS, delay estimation, logical effort, sizing, delay optimization, ratioed logic, pass-transistor logic, dynamic logic

Module 3	**Sequential Logic:** Timing metrics, static latches & registers, dynamic latches & registers, delay constraints & violations, time borrowing, synchronous design, pipelining **Memory:** Classification, architecture, static and dynamic RAMs, non-volatile read-write RAMs, peripheral circuitry, power dissipation
Module 4	**Adders:** Definition, full adder circuit, inverting adder, carry save adder, carry select adder, carry look ahead adder **Multipliers:** Definition, Booth and modified Booth encoding, array multiplier, carry save multiplier, signed multiplication, carry save implementation, final addition
Module 5	**Design flow:** Custom design, semicustom design, array based design. **Interconnects**: Capacitive parasitics, resistive parasitics, inductive parasitics

References:

[1] Jan M. Rabaey, Anantha P. Chandrakasan, and Borivoje Nikolić, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Pearson Education, 2003.

[2] Neil H.E. Weste and David Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed. Addison Wesley, 2015.

[3] David A. Hodges, Horace G. Jackson, and Resve A. Saleh, *Analysis and Design of Digital Integrated Circuits: In Deep Submicron Technology*, Sp. Indian 3 ed. McGraw Hill, 2005.

[4] Ivan Sutherland, Robert F. Sproull, and David Harris, *Logical Effort: Designing Fast CMOS Circuits*. Elsevier Science, 1999.

[5] Sung-Mo Kang and Yusuf Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 4th ed. McGraw-Hill, 2003.

25-509-0103 **Advanced Embedded System Design**

L	T	P	C
3	2	0	3

Prerequisites : Digital design
Course Description : This course introduces the architecture of embedded system using commercially available microcontrollers and platforms.
Course Outcome : After the completion of the course, student will be able to

CO1	Summarize the general architecture of an embedded system	Understand
CO2	Illustrate the architecture of ARM processors	Understand
CO3	Design an embedded system for a given application by interfacing suitable peripherals	Apply
CO4	Describe the architecture of GPU that can be used for building smart systems	Apply

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	2							2
CO2	3			2					2
CO3	3	3						3	2
CO4	3	2		2				2	2

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Introduction:** Overview of general embedded systems - General architecture, Sensors and Actuators, characteristics, Real Life examples : Robotics, Automotive Electronics, Biomedical Applications, Embedded Programming - IDE, Compiler/Assembler, Simulator/Emulator
Module 2	**Processing Element:** Microprocessor, Micro-controller, System on chip (SoC), Digital Signal Processors (DSP), Application Specific IC (ASIC), Field Programmable Gate Arrays (FPGA). Basic concepts of Embedded system design using these elements - Typical architecture of a microcontroller unit by taking ARM Cortex
Module 3	**Overview of Cortex:** Register architecture, Instruction set, GPIO, timer/counter, watch dog timer, Stack, Interrupts, DMA and other peripherals, Debug support, Programming and Design examples of embedded system using ARM Cortex based processors
Module 4	**Smart Embedded Systems :** IoT, Edge Computing, Cyber Physical systems, Example controller - Graphics Processing Unit (GPU)- Programming GPU, Scheduling SIMD threads, NVIDIA GPU architecture, Memory structure

Module 5	**Interfacing Buses and Protocols:** Advanced Microcontroller Bus Architecture (AMBA), Inter-Integrated Circuit (I2C), Serial Peripheral Interphase (SPI), UART, Universal Synchronous Bus (USB), Control Area Network (CAN). Ethernet/WLAN/ Bluetooth/Zigbee. Development Boards - Arduino, LPC1768 ARM Cortex M3, Gelileo, Raspberry, NVDIA Jetson board

References:

[1] Lyla. B. Das, *Embedded Systems, An Integrated Approach.* Pearson Ed, 2013.

[2] John L. Hennessy and David A. Patterson, *Computer Architecture - A Quantitative Approach.* Morgan Kaufmann, 2017.

[3] Jonathan W. Valvano, *RTOS for ARM Cortex-M Microcontrollers.* Createspace Independent Pub, 2017.

[4] Documentation on ARM Cortex processors and develoment boards by ARM.

25-509-0104 Digital System Design Using HDLs Lab

L	T	P	C
0	0	4	2

Prerequisites : Digital design
Lab Description : The lab focuses on design of digital system using HDLs like Verilog and Bluespec. Use front end tools for RTL design and simulations.
Course Outcome : After the completion of the lab, the student will be able to

CO1	Develop basic testbench, simulate and debug Verilog/Bluespec designs using RTL simulation tools	Analyze
CO2	Design combinational and sequential using Verilog/Bluespec HDL	Apply
CO3	Design basic bulding blocks of a processor to realize a simple RISC processor using HDLs	Analyze

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	3	3	3	3	3	3	2	3
CO2	3	2	3	3	3	3	3	2	3
CO3	3	3	3	3	3	3	3	3	3

3-High; 2-Medium; 1-Low

Course Content:

Sample List of Experiments*	
1	Design and simulate : full adder, multiplexer, priority encoder, code convertors, flipflops etc.
2	Design 4-bit adder/code converter using structural, data flow and behavioural models
3	Design of sequential circuits like: counter, shift registers, FIFO, pattern detection etc.
4	Implement 8 bit array multiplier and serial multiplier and compare area, power and delay
5	Design and simulate basic building blocks of processor like register file, ALU, decode unit etc.
6	Design of a simple RISC processor pipeline using the basic building blocks and debug the design using simulations

* The list is not exhaustive. Additional experiments or project based on the experiments can be included in the laboratory activity.

References:

[1] Charles H. Roth Jr., Lizy Kurian John, and Beyeong Kil Lee, *Digital Systems Design Using Verilog*. CL Engineering, 2015.

[2] David Money Harris and Sarah L Harris, *Digital Design and Computer Architecture*. Elsevier, 2019.

[3] Documentation for Cadence, Synopsis and Siemens Front end and Back end tools.

[4] Arvind, Rishiyur S. Nikhil, James C. Hoe, and Silvina Hanono Wachman, "Introduction to digital design as cooperating sequential machines."

[5] Bluespec Reference Guide, "https://web.ece.ucsb.edu/its/bluespec/doc/BSV/reference-guide.pdf."

[6] Stuart Sutherland, Simon Davidmann, and Peter Flake, *SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling*. Springer, 2006.

[7] J. Bhasker, *A Verilog HDL Primer*. Star Galaxy Publishing, 2005.

25-509-0105 **Digital Integrated Circuits Lab**

L	T	P	C
0	0	4	2

Prerequisites : Taken with Digital Integrated Circuit Design
Lab Description : This lab introduces the use of front-end and back-end tools for standard cell based designs.
Course Outcome : After the completion of the lab, the student will be able to

CO1	Characterize speed, energy consumption, and robustness of combinational, sequential, and memory circuits using circuit simulation tools	Analyze
CO2	Draw optimized layouts for standard cells	Apply
CO3	Demonstrate the use of front-end and back-end design tools to obtain optimized layout from RTL models	Apply
CO4	Evaluate different implementation strategies for arithmetic circuits	Evaluate

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3		3	2	2	2	3		3
CO2	3	3	3	2	2	2	3		3
CO3	3		3	2	2	2	3		3
CO4	3	3	3	2	2	2	3	2	3

3-High; 2-Medium; 1-Low

Course Content:

Sample List of Experiments*	
1	MOSFET circuit simualtion and parameter extraction
2	Characterization of static CMOS inverter
3	Characterization of NAND/NOR logic gates
4	Design and analysis of chain of gates
5	Characterization of D flip flops
6	Layout of NAND/NOR standard cell
7	Front end and back end design and analysis of an 8 bit adder
8	Implement 8 bit ripple carry adder and carry look ahead adder and compare area, power and delay

* The list is not exhaustive. Additional experiments or project based on the experiments can be included in the laboratory activity.

References:

[1] Jan M. Rabaey, Anantha P. Chandrakasan, and Borivoje Nikolić, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Pearson Education, 2003.

[2] Documentation for Cadence, Synopsis and Siemens Front-end and Back-end tools.

25-509-0106 **Intelligent Embedded Systems Lab**

L	T	P	C
0	0	4	2

Prerequisites : None
Lab Description : This lab provides experiments to implement embedded systems using development boards, implement intelligent algorithms using neural network and port in edge devices for real work applications.
Course Outcome : After the completion of the lab, the student will be able to

CO1	Familiarise embedded development board and utilise the micro-controller peripherals	Apply
CO2	Integrate sensors and actuators with microcontrollers and implement solutions for problems	Apply
CO3	Solving regression and classification problems using neural network	Apply
CO4	Use neural network for solving real world problems	Apply
CO5	Port intelligent algorithms to embedded edge device for real world problems and analyse the performance	Analyse

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1			3	3	2	2	3	2	3
CO2			3	3	2	2	3	2	3
CO3			3	3	2	2	3	2	3
CO4			3	3	2	2	3	2	3
CO5			3	3	2	2	3	2	3

3-High; 2-Medium; 1-Low

Course Content:

Sample List of Experiments*	
1	Familiarise embedded development board. Utilise the micro-controller peripherals such as Timer, Counter, Interrupts, ADC, GPIO, RTC, UART, I2C. SPI, etc.
2	Integrate sensors and actuators with microcontrollers and implement solutions for problems like temperature monitoring, LCD display, motor control, alarms, communication, etc.
3	Familiarisation of Python, Jupyter notebook and libraries like TensorFlow, Keras, PyTorch, etc for implementing neural network algorithms
4	Model neural networks for Regression tasks and Classification tasks for linear and non-linear data
5	Neural Network models for object detection, image classification, etc.

6	Solution proposal for a real world problem, model a neural network, pre-process the data, train the model and evaluate the performance and improve the learning through parameter tuning. Port the neural network model into an edge embedded system for deployment and analyse the performance

* The list is not exhaustive. Additional experiments or project based on the experiments can be included in the laboratory activity.

References:

[1] Syed R. Rizvi, *Microcontroller Programming.* CRC Press, 2016.

[2] Jon Krohn, *Deep Learning with TensorFlow, Keras, and PyTorch.* Pearson, 2020.

[3] Datasheets of microcontrollers and Documentations of python libraries.

MASTER OF TECHNOLOGY

in

VLSI & EMBEDDED SYSTEMS

Semester 2

DEPARTMENT OF ELECTRONICS

COCHIN UNIVERSITY OF SCIENCE AND TECHNOLOGY

Kochi - 682 022, India

25-509-0201 **Design Verification and Testing**

L	T	P	C
3	2	0	3

Prerequisites : Digital design, Verilog

Course Description : This course deals with the design verification and testing stages of ASIC design flow. It provides an overview of the various components involved in the verification of a digital circuits. It also includes the basic testing and design for testability concepts.

Course Outcome : After the completion of the course, student will be able to

CO1	Summarize the components of design verification environment including coverage and assertion	Understand
CO2	Develop a self checking testbench to verify the given RTL design	Analyze
CO3	Generate test patterns for a circuit considering single-stuck-at fault model	Apply
CO4	Illustrate different design for testability techniques used for digital ICs	Understand

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	3					3	3	2
CO2	3	3					3	3	2
CO3	3	3					3		2
CO4	3	3		3			3	3	2

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Introduction to Verification:** Functional verification versus Formal verification; Testbench; Verification versus Testing; Design and Verification Reuse, The Cost of Verification, Simulation, Waveform Viewers, Code Coverage, Functional Coverage, Assertions, Metrics
Module 2	**Verification Envirnment:** Verification Plan- Levels of Verification, Directed Testbenches Approach, Coverage-Driven Random-Based Approach; High-Level Modeling- Structure of High-Level Code, Race Conditions; Stimulus and Response- Reference Signals, Simple and Complex Stimulus, Bus-Functional Models, Response Monitor
Module 3	**Testbench Architecture:** Design Configuration, Self-Checking Testbenches, Directed Stimulus, Random Stimulus; Transaction-Level Model, Regression, Universal Verification Methodology (UVM)

Module 4	**Fundamentals of VLSI testing:** Fault modeling: Logical fault models, Single Stuck at Faults (SSF), Fault detection, Fault equivalence and fault dominance; Automatic test pattern generation - ATPG for SSF in combinational circuit, D-Algorithm, Sequential ATPG – Time Frame Expansion
Module 5	**Design for testability:** Controllability and Observability, Ad Hoc Design for testability, Generic scan based design, Test interface and boundary scan, Built-in-self- test (BIST)- BIST Architecture, Memory Test-MBIST

References:

[1] Janick Bergeron, *Writing Testbenches using System Verilog.* Springer, 2006.

[2] Charles H. Roth Jr., Lizy Kurian John, and Beyeong Kil Lee, *Digital Systems Design Using Verilog.* C L Engineering, 2015.

[3] Michael L. Bushnell and Vishwani D. Agrawal, *Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits.* Springer, 2005.

[4] Miron Abramovici, Melvin A. Breuer, and Arthur D. Friedman, *Digital System Testing and Testable Design.* IEEE Press, 1994.

[5] Chris Spear and Greg Tumbush, *System Verilog for Verification.* Springer, 2012.

[6] Stuart Sutherland, Simon Davidmann, and Peter Flake, *SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling.* Springer, 2006.

25-509-0202 **FPGA Based Embedded SoC Design**

L	T	P	C
3	2	0	3

Prerequisites : Digital design basics
Course Description : This course presents basic FPGA architectures and FPGA SoC architectures. Implementation of embedded systems on FPGA SoCs is also covered.
Course Outcome : After the completion of the course, student will be able to

CO1	Summarize architectural features of various types of FPGAs	Understand
CO2	Model hardware blocks for optimized implementation on FPGAs	Apply
CO3	Explain different blocks in FPGA SoCs	Understand
CO4	Illustrate the concepts involved in system design on FPGAs	Apply
CO5	Discuss the different steps in SoC Design	Understand

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3						3		
CO2	3	3					3		
CO3	3						3		
CO4	3	3					3	2	
CO5	3		2				3		2

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**FPGA Overview:** Introduction, requirements & specification, hierarchical design, design abstraction **FPGA Architecture:** SRAM based FPGAs, permanently programmable FPGAs, I/O, circuit design & architecture of FPGA fabrics, carry chains and cascade chains, design flow, Case study: Xilinx 7-series architecture
Module 2	**Hardware Design & Optimization:** Modeling combinational logic using HDLs, combinational network delay, power and energy optimization, logic implementation, physical design, sequential design styles, clocking rules, architecting for speed, area and power, Case study - AES
Module 3	**FPGA SoCs:** Buses - AMBA & AXI, platform FPGA architectures, high speed transceivers, clocks, embedded memories & arithmetic blocks, creating IP blocks, soft core & hard core processors, Case Study: Xilinx Zync 7000 SOC **Clocks & Resets:** Crossing clock domains, gated clocks, asynchronous vs synchronous resets, Case study - I2S

Module 4	**System Design:** Principles, control flow graphs, hardware design, software design, debugging, Partitioning - analytical solution, communication, practical issues, Parallelism - principles, identifying parallelism, spatial parallelism, Bandwidth - techniques, scalable designs, on-chip and off-chip memory access
Module 5	**SoC Design:** SoC Overview, taxonomy of ICs, design abstraction, design flow, behavioral synthesis, scheduling, binding, resource sharing, on-chip communication architecture, modeling & co-simulation, hw/sw partitioning & co-synthesis, Case study - example using Xilinx Vivado HLS

References:

[1] Wayne Wolf, *FPGA Based System Design.* Prentice Hall PTR, 2004.

[2] Steve Kilts, *Advanced FPGA Design Architecture, Implementation, and Optimization.* Wiley-IEEE Press, 2007.

[3] Ron Sass and Andrew G. Schmidt, *Embedded Systems Design with Platform FPGAs, Principles and Practices.* Elsevier, 2007.

[4] Charles H. Roth Jr., Lizy Kurian John, and Beyeong Kil Lee, *Digital Systems Design Using Verilog.* Elsevier, 2007.

[5] Xilinx FPGA user guides and documentation.

25-509-0203 **Design Verification and Testing Lab**

L	T	P	C
0	0	4	2

Prerequisites : Digital design, Verilog
Lab Description : The lab will provide hands-on experience on implementing a test-bench to verifying a given digital design. This will also include exposure to testing tool for scan insertion and ATPG.
Course Outcome : After the completion of the lab, the student will be able to

CO1	Develop a test plan for a given specification	Analyze
CO2	Design functional verification environment for a Verilog RTL that can achieve the target coverage	Evaluate
CO3	Perform gate level timing simulation of netlist post and pre-layout	Apply
CO4	Stitch scan and generated test pattern for desired coverage using tools	Apply

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	3	3	3	3	3	3	3	
CO2	3	3	3	3	3	3	3	3	3
CO3	3	3	3	3	3	3	3	3	3
CO4	3	3	3	3	3	3	3	3	3

3-High; 2-Medium; 1-Low

Course Content:

Sample List of Experiments*	
1	Familiarise the components of functional verification environment using simple components like full adder, multiplexer etc.
2	Functional verification of 4-bit adder with code/functional coverage
3	Functional verification of 8-bit counter with code/functional coverage
4	Functional verification of a simple RISC processor with code/functional coverage
5	Generate a gate level netlist of the given RTL and complete the physical design flow to extract timing parameters
6	Insert scan in the given netlist and generate test pattern to get 100% coverage
7	Gate level simulation post and pre-scan insertion

* The list is not exhaustive. Additional experiments or project based on the experiments can be included in the laboratory activity.

References:

[1] Janick Bergeron, *Writing Testbenches using System Verilog.* Springer, 2006.

[2] Charles H. Roth Jr. , Lizy Kurian John, and Beyeong Kil Lee, *Digital Systems Design Using Verilog.* C L Engineering, 2015.

[3] David Money Harris and Sarah L. Harris, *Digital Design and Computer Architecture.* Elsevier, 2019.

[4] Michael L. Bushnell and Vishwani D. Agrawal, *Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits.* Springer, 2005.

[5] Chris Spear and Greg Tumbush, *System Verilog for Verification.* Springer, 2012.

[6] Ray Salemi, *Python for RTL Verification: A complete course in Python, cocotb, and pyuvm.* Amazon Digital Services LLC, 2022.

[7] Documentation for Cadence, Synopsis and Siemens Front end and Back end tools.

MASTER OF TECHNOLOGY

in

VLSI & EMBEDDED SYSTEMS

Semester 3

DEPARTMENT OF ELECTRONICS

COCHIN UNIVERSITY OF SCIENCE AND TECHNOLOGY

Kochi - 682 022, India

25-509-0301 **PROJECT : PART 1**

L	T	P	C
0	0	28	14

Prerequisites : None
Course Description : This is the first part of the final project.
Course Outcome : After the completion of the course, the student will be able to

CO1	Identify unresolved problems and challenges in the selected domain through literature survey	Analyze
CO2	Determine appropriate tools and procedures for design, development & verification	Evaluate
CO3	Develop practical solutions for the chosen problem for a given specification	Create
CO4	Develop the ability to write good technical report, to make oral presentation of the work, and to publish the work in reputed conferences/journals	Create

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3			3	3	3	3		
CO2	3	3	3	2	2	3	3		3
CO3	3	3	3	2	2	3	3	3	3
CO4				3	3	3			

3-High; 2-Medium; 1-Low

Course Content:

The major project in the third and fourth semesters offer the opportunity to apply and extend knowledge acquired in the first year of the M. Tech. program. The major project can be analytical work, simulation, hardware design or a combination of these in the emerging areas of VLSI & Embedded Systems under the supervision of a faculty from the Dept. of Electronics or in R and D institutes/ Industry. The specific project topic undertaken will reflect the common interests and expertise of the student(s) and supervisor. Students doing their project outside the department will be assigned an internal supervisor.

Students will be required to

- perform a literature search to review current knowledge and developments in the chosen technical area
- undertake detailed technical work in the chosen area using one or more of the following:
  - Analytical models
  - Computer simulations
  - Hardware implementation

The emphasis of major project shall be on facilitating student learning in technical, project management and presentation spheres. Project work will be carried out individually. The project supervisor/internal supervisor shall do monthly evaluation of the progress. M. Tech project evaluation committee for the course shall evaluate the project work during the third semester in two stages. The first evaluation shall be conducted in the middle of the semester. This should be followed by the end semester evaluation. By the time of the first evaluation, students are expected to complete the literature review, have a clear idea of the work to be done, and have learnt the analytical / software / hardware tools. By the time of the second evaluation, they are expected to present the results of their advancements in the chosen topic, write an interim technical report of the study and results and clearly state the work plan for the next semester.

25-509-0302 **MOOC/NPTEL Course**

L	T	P	C
			2

Prerequisites : None
Course Description : This course has to be completed through MOOC mode using NPTEL/SWAYAM or other university approved MOOC platforms.
Course Outcome : After the completion of the course, the student will be able to

CO1	Demonstrate the ability for independent learning	Apply
CO2	Follow ethical practices for timely submissions	Apply

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3			3	3	3	3		
CO2				3	3	3			

3-High; 2-Medium; 1-Low

Course Content:

Massive Open Online Courses (MOOCs) are free online courses available for anyone to enroll.MOOCs provide an affordable and flexible way to learn new skills, advance your career and deliver quality educational experiences at scale. The students have to complete a minimum 8 week duration course which will yield them a credit of 2. The selection of the course will be dependent on their specialisation and should be approved by the committee constituted for the same. The modality of the course will be as per the university guidelines on MOOC courses.

MASTER OF TECHNOLOGY

in

VLSI & EMBEDDED SYSTEMS

Semester 4

DEPARTMENT OF ELECTRONICS

COCHIN UNIVERSITY OF SCIENCE AND TECHNOLOGY

Kochi - 682 022, India

25-509-0401 **PROJECT : PART 2**

L	T	P	C
0	0	32	16

Prerequisites : Successful completion of 25-509-0301 Project: Part 1
Course Description : This is the second and final part of the final project.
Course Outcome : After the completion of the course, the student will be able to

CO1	Identify unresolved problems and challenges in the selected domain through literature survey	Analyze
CO2	Determine appropriate tools and procedures for design, development & verification	Evaluate
CO3	Develop practical solutions for the chosen problem for a given specification	Create
CO4	Develop the ability to write good technical report, to make oral presentation of the work, and to publish the work in reputed conferences/journals	Create

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3			3	3	3	3		
CO2	3	3	3	2	2	3	3		3
CO3	3	3	3	2	2	3	3	3	3
CO4				3	3	3			

3-High; 2-Medium; 1-Low

Course Content:

Project: Part 2 is a continuation of Project: Part 1 in the third semester. Students should complete the work planned in the third semester, attaining all the objectives, and should prepare the project report of the complete work done in the two semesters. They are expected to communicate their innovative ideas and results in reputed conferences and/or journals. The project supervisor/internal supervisor shall do monthly evaluation of the progress. The M. Tech. project evaluation committee of the department shall evaluate the project work during the fourth semester in two phases. The first evaluation shall be conducted towards the middle of the semester. This shall be followed by the end semester evaluation by the committee.

MASTER OF TECHNOLOGY

in

VLSI & EMBEDDED SYSTEMS

Electives

DEPARTMENT OF ELECTRONICS

COCHIN UNIVERSITY OF SCIENCE AND TECHNOLOGY

Kochi - 682 022, India

25-509-0X11 **VLSI Technology**

L	T	P	C
3	1	0	3

Prerequisites : None
Course Description : This course impart an in-depth knowledge of the wafer preparation methods, details of VLSI processing steps and isolation techniques used in VLSI fabrication.
Course Outcome : After the completion of the course, student will be able to

CO1	Understand the wafer preparation methods and the concept of clean room	Understand
CO2	Analyse the deposition, epitaxy, and oxidation methods	Analyze
CO3	Understand etching and diffusion mechanisms in semiconductors	Understand
CO4	Understand ion implantation and isolation techniques used in VLSI fabrication	Understand
CO5	Analyse integration processes and packaging technologies	Analyze

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	3					2		
CO2	3	3	3	3			3		
CO3	3	3		3			3	3	
CO4	3	3		3			2	2	
CO5	3	3					3		

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Semiconductor Crystal Growth and Wafer Engineering:** Historical perspective, semiconductor manufacturing, processing overview, Crystal growth- Electronic grade silicon, Czochralski growth, Bridgman growth, Float zone growth, Si wafer characterization and properties of Silicon wafers, clean rooms, gettering and wafer cleaning
Module 2	**Deposition:** Deposition- Thin films deposition, evaporation, E-beam and resistive heating evaporation, Sputtering, PLD and chemical vapor deposition **Epitaxy and Oxidation:** Molecular beam epitaxy, vapor phase epitaxy, liquid phase epitaxy, ALD, evaluation of epitaxial layers. silicon oxidation-Thermal oxidation process, kinetics of growth, Deal-Grove model, properties of Silicon dioxide, oxide quality, high K and low K dielectrics

Module 3	**Lithography and Diffusion:** Lithography - photo-reactive materials, pattern generation and mask making, pattern transfer, photolithography, electron beam, Ion beam and X-ray lithography- Etching- Wet and dry etching, reactive ion etching, plasma and ion beam techniques.Diffusion-Diffusion process, modeling of diffusion, diffusion in a concentration gradient, impurity behaviour, diffusion systems, problems in diffusion, evaluation of diffused layers
Module 4	**Ion Implantation:** Types Ion Implantation, modeling of Ion implantation, penetration range, Ion implantation systems, process considerations, implantation damage and rapid thermal annealing Device Isolation - Junction and oxide isolation, LOCOS, shallow trench isolation, contacts and Metallization-Schottky contacts, ohmic contacts, planarization techniques
Module 5	**Integration of processes for bipolar :** N well, P-well and Twin tub CMOS, BiCMOS fabrication processes -Defining system rules for IC layout - Packaging - Diebonding, wire-bonding, flip-chip technology - Future trends and challenges- Challenges for integration, system on chip

References:

[1] Sorab K. Ghandhi, *VLSI Fabrication principles*. John Wiley Inc, 2008.

[2] S. M. Sze, *VLSI Technology*, 4th ed. McGraw Hill Co. Inc, 2017.

[3] James D. Plummer, Michael D. Deal, and Peter B. Griffin, *Silicon VLSI Technology*. Prentice Hall Electronics, 2010.

[4] Richard C. Jaeger, *Introduction to microelectronic fabrication*, 2nd ed. Prentice Hal, 2013.

[5] C. Y. Chang and S. M. Sze, *VLSI Technology*. McGraw Hill Co. Inc., New York, 1996.

[6] Stephen A. Campbell, *The Science and Engineering of Microelectronic Fabrication*, 4th ed. Oxford University Press, 1996.

25-509-0X12 **VLSI Design Automation**

L	T	P	C
3	1	0	3

Prerequisites : None
Course Description : To explore the principles and techniques for automating the design and optimization of integrated circuits to enhance efficiency and productivity in the semiconductor field.
Course Outcome : After the completion of the course, student will be able to

CO1	Understand the basic graph algorithms, optimizations and design styles used in digital IC designs	Understand
CO2	Understand placement and partitioning algorithms	Understand
CO3	Apply the floor planning concepts to compute the optimal shape of the circuit	Apply
CO4	Interconnect the cells to the positions assigned by placement	Apply
CO5	Map the behavioral description at the algorithmic level to a structural description	Apply
CO6	Review the recents trends and developments in VLSI design automation	Understand

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3		2				2		2
CO2	3		2				3		2
CO3	3	3	2				3		2
CO4	3	3	2				3		2
CO5	3	3	2				3		2
CO6	3		2	2			3		2

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Introduction to digital IC design:** VLSI Design Cycle, Physical Design Cycle, Design Styles-Full custom, standard cell, gate array, FPGA. Design problem, design domains, Introduction to VLSI design automation tools. Graph algorithms – Depth-first search, Breadth-first search, Dijikstra‘s shortest path algorithm, Prim‘s algorithm. Combinatorial optimization problems, decision problems, NP-completeness, NP-hardness, backtracking, branch and bound, dynamic programming, inter linear programming

Module 2	**Partitioning:** Simulated annealing and evolution.Algorithms for constraint-graph compaction, standard cell placement and building block placement. Partitioning - Constructive and iterative algorithms - Kernighan-Lin algorithm - Fiduccia-Mattheyses algorithm – Goldberg-Burstein Algorithm - Multilevel partitioning, clustering
Module 3	**Floor planning and Placement:** Slicing and non-slicing floor plan - Polish expression - Constraint-based, analytical, rectangular dual graph, hierarchical tree methods - Pin assignment – General and channel pin assignment – Placement – Cost function – Simulation, partitioning and performance based placement algorithms
Module 4	**Routing:** Global routing - Maze routing, line search, Steiner tree based algorithms – Detailed routing–Constraint graphs – Channel routing - Left edge algorithm – Dog leg routing – Switch box routing – Over the cell routing – Clock network design considerations - Clock tree synthesis - Power and ground routing - Static timing analysis and timing closure
Module 5	**High Level Synthesis:** Allocation assignment and scheduling, Simple scheduling, algorithm level transformations **Current trends:** CAD for 2.5D/3D integration, CAD for Novel Semiconductor Devices based designs, Machine Learning/AI driven EDA etc.

References:

[1] Sabih H. Gerez, *Algorithms for VLSI Design Automation*. John Wiley & Sons, 2006.

[2] Naveed A. Sherwani, *Algorithms for VLSI Physical Design Automation*, 3rd ed. Springer, 2013.

[3] Andrew B. Kahng, Jens Lienig, Igor L. Markov, and Jin Hu, *VLSI Physical Design: From Graph Partitioning to Timing Closure*. Springer Netherlands, 2011.

[4] Laung-Terng Wang, Yao-Wen Chang, and Kwang-Ting (Tim) Cheng, *Electronic Design Automation: synthesis, verification, and test*. Morgan Kaufmann, 2009.

[5] Sadiq M. Sait and Habib Youssef, *VLSI Physical Design Automation: Theory and Practice*. World Scientific, 1999.

[6] Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, and Clifford Stein, *Introduction to Algorithms*, 4th ed. The MIT Press, 2022.

[7] Recent articles from IEEE Transactions on Very Large Scale Integration (VLSI) Systems and IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.

25-509-0X13 **Low Power VLSI**

L	T	P	C
3	1	0	3

Prerequisites : MOSFET basics, digital circuits
Course Description : This course introduces students to power reduction techniques at different levels of abstraction of digital design flow.
Course Outcome : After the completion of the course, student will be able to

CO1	Discuss circuit level optimizations and leakage reduction techniques	Understand
CO2	Perform gate level and RTL level optimizations for dynamic power reduction	Apply
CO3	Design the different components and IPs for power gated designs	Apply
CO4	Explain the techniques applied for frequency and voltage scaling designs	Understand
CO5	Summarize the different stages in the design flow for multi-voltage, power gated designs	Understand

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3						3		
CO2	3	2					3		
CO3	3	2					3		
CO4	3						3		
CO5	3		2				3		2

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Introduction:** Static, dynamic and leakage power dissipation, power vs. energy, limits of low power VLSI designs **Circuit level optimizations:** Transistor and gate sizing, optimal supply voltage, pin reordering, network restructuring, special latches and flip flops **Leakage Reduction Techniques:** Transistor stacks, power gating, multi-threshold CMOS, variable threshold CMOS, dynamic threshold CMOS

Module 2	**Gate Level Optimizations:** Minimizing switched capacitance, switching activity reduction, gate reorganising, signal gating, logic encoding, state machine encoding, precomputation logic, clock gating, reducing glitching through path balancing, input reordering **RTL & Block Level Optimizations:** RTL coding for low power, glitch reduction, clock gating, gated clock FSM, bus encoding, clock control, clock skew, input control
Module 3	**Designing Power Gating:** Power switching – fine grain vs. coarse grain, switching fabric design, signal isolation, state retention and restoration methods, power gating control, power networks and their control, power state tables and always on regions, case study **IP Design for Low Power:** Architecture and partitioning for power gating, power controller design example- issues, clocks and resets, verification. packaging IP for reuse with power intent, unified power format(UPF) examples
Module 4	**Frequency & Voltage Scaling:** Voltage scaling interfaces- level shifters, timing issues in multi-voltage designs, voltage scaling approaches, dynamic voltage and frequency scaling (DVFS), CPU subsystem design issues, adaptive voltage scaling (AVS), level shifters and isolation, voltage scaling interfaces - effect on synchronous timing, control of voltage scaling, examples of voltage and frequency scaling design
Module 5	**Design Flow for Multi-Voltage, Power Gated Designs:** Overview, partitioning, synthesis, multi corner multi mode optimization, design planning, power planning, clock tree synthesis, power analysis, timing analysis, low power validation, manufacturing test **Physical Libraries:** Standard cell libraries, isolation cells, level shifters, memories, power gating strategies and structures, power gating cells, power gated standard cell libraries, retention registers, memory retention methods

References:

[1] Michael Keating, David Flynn, Robert Aitken, Alan Gibbons, and Kaijian Shi, *Low Power Methodology Manual For System-on-Chip Design*, 1st ed. Springer New York, NY, 2007.

[2] Roy Kaushik and Sharat C. Prasad, *Low-power CMOS VLSI circuit design*, Wiley Student ed. John Wiley & Sons, 2009.

[3] Gary K. Yeap, *Practical low power digital VLSI design.* Springer Science & Business Media, 2012.

[4] Abdellatif Bellaouar and Mohamed Elmasry, *Low-power digital VLSI design: circuits and systems.* Springer Science & Business Media, 2012.

[5] Christian Piguet, *Low-power CMOS circuits: technology, logic design and CAD tools.* CRC Press, 2005.

[6] Jan M. Rabaey, Anantha P. Chandrakasan, and Borivoje Nikolić, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Pearson Education, 2003.

25-509-0X14 **Neural Networks**

L	T	P	C
3	1	0	3

Prerequisites : None
Course Description : This course provides a broad overview to neural networks and its optimisation algorithm, heuristics and model analysis.
Course Outcome : After the completion of the course, student will be able to

CO1	Concept of learning, architectures and mathematical modelling of neuron	Understand
CO2	Model a linear regressor and classifier using a perceptron	Apply
CO3	Solve non-linear problems using multi-layer neural network	Apply
CO4	Analyse model performance and implement better training algorithms for neural network	Analyse
CO5	Understand RBFN networks and how to solve non-linear problems with kernel functions	Understand

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3						3		
CO2	3	2	2				3	2	2
CO3	3	2	2				3	2	2
CO4	3	2	2				3	2	2
CO5	3						3		

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Introduction:** Motivation from Human Brain, mathematical model of a neuron, basic computational unit, Activation Functions, Neural networks viewed as Directed Graphs, Feedback, Network Architectures, Knowledge Representation. Learning Process–Supervised, Unsupervised and Reinforcement learning, Learning Tasks-Pattern Association, recognition, function approximation, control, beamforming
Module 2	**Perceptron:** Perceptron convergence theorem, Relation between perceptron and Bayes classifier for a Gaussian Environment, batch perceptron algorithm. Model building through regression- linear regression model, Cost Function, learning rate, gradient descent algorithm, chain rule, optimization, Local minima, Global Minima, computer experiment: regression and pattern classification. Least-Mean-Square Algorithm

Module 3	**Multilayer Perceptron:** XOR problem, hidden layer, non-linearity, Back propagation algorithm, local error gradients, Back propagation and differentiation, Hessian matrix, optimal annealing and adaptive control of the learning rate, Approximations of function, Generalization, Cross validation, Network pruning Techniques, Optimal Brain Surgeon, Virtues and limitations of back propagation learning. computer experiment: pattern classification
Module 4	**Heuristics:** Heuristics for making the back-propagation algorithm perform better, batch learning and stochastic learning, activation functions, differentiability, symmetric, feature scaling, initialization, learning rate, momentum term, stopping criteria, Learning Curves, Early Stopping, Evaluation Measures: Training, Validation, Testing. Two class evaluation measures, Confusion Matrix
Module 5	**Radial-Basis Function networks:** Cover's theorem on the separability of patterns, the interpolation problem, radial-basis-function networks, k-means clustering, recursive least-squares estimation of the weight vector, hybrid learning procedure for RBF networks, computer experiment: pattern classification, interpretations of the Gaussian hidden units

References:

[1] Simon Haykin, *Neural Networks and Learning Machines*, 3rd ed. Pearson Education India, 2016.

[2] Martin T. Hagan, Howard B. Demuth, Mark H. Beale, and Orlando De Jesús, *Neural Network Design*, 2nd ed. Cengage Learning, 2014.

[3] Simon Haykin, *Neural Networks: A Comprehensive Foundation*, 2nd ed. Prentice Hall, 1999.

[4] Philip D. Wasserman, *Neural Computing: Theory and Practice*. Coriolis Group, 1989.

[5] B. Yegnanarayana, *Artificial neural networks*. Prentice Hall of India, 2005.

[6] James A. Freeman and David M. Skapura, *Neural Networks Algorithms, Applications and. Programming Techniques*. Pearson Education, 2002.

25-509-0X15 **Analog & RF IC Design**

L	T	P	C
3	1	0	3

Prerequisites : Circuit analysis

Course Description : This course introduces students to the analysis and design of basic analog integrated circuit components like amplifiers, current mirrors and biasing circuits. Specifications and trade-offs involved in analog design are covered. The course also covers various factors involved in the design of RF integrated circuit components.

Course Outcome : After the completion of the course, student will be able to

CO1	Perform small signal analysis using MOSFET models	Apply
CO2	Design single stage and differential amplifiers for given specification	Apply
CO3	Discuss about appropriate current sources and voltage references for biasing	Undersatnd
CO4	Understand the basic building blocks of RF ICs and the trade-offs involved in RF designs	Understand
CO5	Explain the methodologies for designing RF IC components with given specifications	Undersatnd

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	3					3		
CO2	3	3					3		
CO3	3						3		
CO4	3						3		
CO5	3						3		

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Introduction:** Review of 4 terminal MOSFET, small signal model and analysis, high frequency model **RF Basic Concepts:** Non linearity and its effects, noise, sensitivity & dynamic range, passive impedance transformation, scattering parameters, bandwidth estimation techniques
Module 2	**Single Stage Amplifiers:** Single stage amplifiers - common source, source follower, common gate, cascode amplifiers, frequency response, noise

Module 3	**Differential Amplifiers:** Basic differential pair, common mode response, frequency response, noise, MOS transistor mismatch, effect of transistor mismatch **Current Mirrors & Biasing:** Basic and cascode current mirrors, effect of transistor mismatch, biasing techniques, self biasing circuits, supply independent bias circuits, bandgap reference
Module 4	**Low Noise Amplifiers:** Input matching, LNA topologies, gain and band switching, non linearity calculations, power constrained design optimizations, design examples **Mixers:** Mixer fundamentals, mixing using non linear systems, multiplier based mixers
Module 5	**Oscillators:** Ring oscillators, LC oscillators, inductors and capacitors, voltage controlled oscillators **Phase Locked Loops**: Simple PLL, Type II PLL, Non-idealities, phase noise

References:

[1] Behzad Razavi, *Design of Analog CMOS Integrated Circuit*, 2nd ed. McGraw Hill India, 2017.

[2] Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge University Press, 2014.

[3] Behzad Razavi, *RF Microelectronics*, 2nd ed. Prentice Hall, 2012.

[4] Phillip E. Allen and Douglas R. Holberg, *CMOS Analog Circuit Design*, 3rd ed. Oxford University Press, 2013.

[5] Jacob Baker R., *CMOS Circuit Design, Layout and Simulation*, 3rd ed. Wiley-Blackwell, 2010.

25-509-0X16 **Robotics Technology**

L	T	P	C
3	1	0	3

Prerequisites : None
Course Description : This course provides an overview of Robot mechanisms for the design and control of robotic systems.
Course Outcome : After the completion of the course, student will be able to

CO1	Apply the mathematics of spatial descriptions and transformations and determine the kinematic equation of the manipulator	Apply
CO2	Illustrate the concept of singularity by calculating the Jacobian of a manipulator and Derive kinetic and potential energy in a robot manipulator	Apply
CO3	Discuss about the basics of locomotion, kinematics, dynamics and motion control of mobile robots	Understand
CO4	Determine appropriate localization strategies for mobile robots based on the perception capabilities	Apply
CO5	Learn different motion planning, navigation schemes and the latest developments in mobile robotics	Understand

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	3					2		
CO2	3	3	3	3			3		
CO3	3	3		3			3	3	
CO4	3	3		3			2	2	
CO5	3	3					3		

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Introduction to robotics, transformations, and Kinematics:** Brief history, types and applications of robots, robot configurations and concept of workspace, types of actuators and sensors in robotics, types of grippers. Basics of kinematics, coordinate frames and transformations, homogenous transformations, kinematics parameters, D-H representation, Arm equation, Inverse Kinematics
Module 2	**Serial robotic manipulator dynamics:**Velocity propagation from link to link, Jacobian, singularities; static forces in manipulators; Jacobians in force domain, Newton-Euler dynamic formulation; Lagrange-Euler formulation, dynamic equations for multiple degrees of freedom robot

Module 3	**Introduction to Mobile robots:** Key issues for locomotion, Legged Mobile Robots, Wheeled Mobile Robots **Kinematics, Dynamics and Motion Control of mobile robots:** Kinematic Models and Constraints of wheeled mobile robot, Forward kinematic models, Wheel kinematic constraints, Robot kinematic constraints, Mobile Robot Maneuverability, Mobile Robot Workspace, Mobile Robot Workspace, Dynamics and motion controlling methods
Module 4	**Perception:**Proprioceptive/Exteroceptive and passive/active sensors, Performance measures of sensors, Wheel/motor sensors, Representing uncertainty, Error propagation: combining uncertain measurements, Feature extraction **Localization:** Introduction - Challenges, Odometric position estimation, Belief representation, Map representation, map based localization, Probabilistic rap-based Localization, Markov localization, Autonomous map building, SLAM
Module 5	**Motion Planning and Navigation:** Path planning, graph search methods, potential field planning, path planning algorithms based on Breadth-first, Depth-first, Dijkstra, A-star, rapidly exploring random trees, Obstacle avoidance **Introduction to modern mobile robots:** Swarm robots, cooperative and collaborative robots, mobile manipulators, autonomous mobile robots

References:

[1] King-Sun Fu, C.S.George Lee, and Ralph Gonzalez, *Robotics: Control, Sensing, Vision and Intelligence*. McGraw-Hill, 1987.

[2] Mark W. Spong and M. Vidyasagar, *Robot Dynamics and Control*. Wiley, 2008.

[3] Roland Siegwart, Illah Reza Nourbakhsh, and Davide Scaramuzza, *Introduction to Autonomous Mobile Robots*. MIT Press, USA, 2011.

[4] H. R. Everett, *Sensors for Mobile Robots – Theory and Applications*. A. K. Peters Ltd., 1995.

[5] Thomas R. Kurfees, *Robotics and Automation Handbook*. CRC Press, 2004.

[6] Johann Borenstein, *Where am I? Sensors and Methods for Mobile Robot Positioning*. The University of Michigan, 1996.

25-509-0X17 Device Physics and Modeling for Integrated Circuits

L	T	P	C
3	1	0	3

Prerequisites : None
Course Description : This course reviews and strengthens the understanding of device physics studied at undergraduate level and provides indepth discussions on short channel MOSFETs and advanced MOS devices. The course also covers circuit level modeling of MOS devices.
Course Outcome : After the completion of the course, student will be able to

CO1	Apply fundamental physics to model PN junctions and metal semiconductor junctions	Apply
CO2	Model the characteristics of MOS devices	Apply
CO3	Employ appropriate models to analyze and characterize MOSFET circuits	Apply
CO4	Explain the physics behind advanced FETs	Understand

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	3	2				3		2
CO2	3	3	2				3		2
CO3	3	3	2				3		2
CO4	3						3		

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Semiconductor fundamentals:** Band model for solids, carrier concentrations, transport, generation-recombination, excess carriers **P-N junctions:** potential barrier, quasi-neutrality, reverse biased junction, breakdown, static and dynamic behavior, small signal and large signal models, SPICE model, simulation exercises using TCAD
Module 2	**Metal-semiconductor junction:** Band diagram, depletion region, capacitance, Schottky barrier, I-V characteristics, Ohmic contacts, TCAD exercises **MOS Capacitor:** Basic physics and analysis, equilibrium and non-equilibrium, C-V characteristics, oxide and surface charges, TCAD exercises
Module 3	**MOS Transistors:** Long-channel MOSFET - basic physics and models, channel-length modulation, body effect, sub threshold regime, small signal model, short and narrow channel effects, radiation and hot-carrier effects, parameter extraction, Spice Models, BSIM model, TCAD exercises

Module 4	**Complementary MOS:** Design considerations, latchup, digital design quality metrics, transient response, switch model, interconnect models, Elmore delay model, sequential circuit timing parameters, MOSFET Scaling
Module 5	**Modern MOSFETs:** High-k dielectrics, metal gates, strain, silicon-on-insulator, FINFETs **Nanoscale MOSFETs**: Basic theory, ballistic transport, scattering, nanowire and carbon nanotube transistors

References:

[1] Theodore I. Kamins and Richard S. Muller, *Device Electronics for Integrated Circuits*, 3rd ed. Wiley, 2002.

[2] Yannis Tsividis and Colin McAndrew, *Operation and Modeling of the MOS Transistor*, 3rd International ed. OUP USA, 2012.

[3] Jan M. Rabaey, Anantha P. Chandrakasan, and Borivoje Nikolić, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Pearson Education, 2003.

[4] Chenming Hu, *Modern Semiconductor Devices for Integrated Circuits*, 1st ed. Prentice Hall, 2010.

[5] Mark S. Lundstrom and Jing Guo, *Nanoscale Transistors: Device Physics, Modeling and Simulation*, 1st ed. Springer US, 2006.

[6] Sung-Mo (Steve) Kang and Yusuf Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 2nd ed. McGraw-Hill, 2003.

[7] J. P. Colinge, *FinFETs and Other Multi-Gate Transistors*. Springer, 2008.

[8] Mark Lundstrom. (2008) Physics of Nanoscale MOSFETs. 2/3/2024. [Online]. Available: https://nanohub.org/resources/5306#series

[9] Sentaurus TCAD Documentation Synopsys Inc. 2/3/2024. [Online]. Available: https://www.synopsys.com/manufacturing/tcad/device-simulation/sentaurus-device.html

25-509-0X18 **Advanced Computer Architectures**

L	T	P	C
3	1	0	3

Prerequisites : Digital design
Course Description : This course provides an insight in the design of high-end microprocessors that support modern applications.
Course Outcome : After the completion of the course, student will be able to

CO1	Design RISC-V processors with performance optimization and hazard avoidance techniques	Apply
CO2	Understand the various optimizations in memory and build a memory hierarchy	Apply
CO3	Compare the performance of various techniques that make use of instruction level parallelism	Analyze
CO4	Illustrate vector and graphics processor architectures that exploit data level parallelism to achieve high performance	Understand

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	3					3	3	
CO2	3	3					3	3	
CO3	3	3					3	3	
CO4	3	3		2			3	3	

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Review of basics:** Von-Neumann architecture, Concept of memory and addressing. Performance measurement- IPC, CPI, benchmarks. Speed-up Law. RISC vs CISC architectures, RISC-V instruction set architecture (ISA) - classification, addressing modes, instruction set encoding, assembly language syntax and convention, RISC-V pipeline architecture - Performance, Pipeline hazards and analysis, Branch Prediction
Module 2	**Memory Hierarchy:** Locality of reference, Cache - Performance, Mapping, Identification, Cache Replacement, Write Strategy, Types of misses, Cache optimizations, Virtual memory concepts - Address Translations, Page tables, TLB, DRAM system- Organization, Memory controllers, DRAM refresh circuitry and power managements schemes, DRAM scheduling

Module 3	**RISC-V Architecture:** Interrupts and exceptions handling, Privilege levels and protection mechanisms, System calls and operating system interface, interrupt controllers and device drivers. Pipelined processor design using RISC-V ISA, performance analysis and evaluation. RISC-V Tools Ecosystem - assemblers, compilers, and linkers, simulation and debugging tools, development boards and platforms, software development and debugging. RISC-V extensions, Case study of RISC-V based processor design
Module 4	**Instruction Level Parallelism:** Compiler techniques to exploit ILP, pipeline scheduling, loop unrolling, advanced branch prediction schemes, dynamic scheduling, Tomasulo's approach, hardware base speculation, VLIW approach for multi-issue, advanced pipelining, superscalar processors and super pipelining
Module 5	**High Performance Computing:** Fine-grained multithreading, Coarse-grained multithreading, Shared-Memory Architectures- Centralized, Distributed, Coherence protocols, Models of Memory Consistency, Tiled chip Multicore processor, Data Level Parallelism - Vector architectures and GPU architecture

References:

[1] John L. Hennessy and David A. Patterson, *Computer Architecture - A Quantitative Approach.* Morgan Kaufmann, 2017.

[2] Bruce Jacob, Spencer W. Ng, and David T. Wang, *Memory System-Cache, DRAM and Disk.* Morgan Kaufman, 2007.

[3] David A. Patterson and John L. Hennessy, *Computer Organization and Design,The Hardware/Software interface: RISC-V Edition* . Morgan Kaufman, 2017.

[4] William Stallings, *Computer Organization and Architecture.* Pearson Ed, 2022.

[5] Dezso Sima, Terence Fountain, and Peter Kacsuk, *Advanced Computer Architectures-A Design Space Approach.* Pearson, 2002.

[6] "RISC-V International," https://riscv.org/.

[7] "Shakthi Processors," https://shakti.org.in/.

[8] "Vega Processors," https://vegaprocessors.in/.

25-509-0X19 **Deep Neural Network Signal Processing**

L	T	P	C
3	1	0	3

Prerequisites : Neural Networks
Course Description : This course provides an overview to various deep neural network architectures and algorithms for spatial and temporal signal processing.
Course Outcome : After the completion of the course, student will be able to

CO1	Model convolution network based feature extraction and prediction	Apply
CO2	Model recurrent networks for temporal and sequential signals	Apply
CO3	Model encoder-decoder networks for spatial/temporal signals	Apply
CO4	Understand generative networks and adversarial learning methods	Understand
CO5	Understand the regularization of deep neural networks and strategies for better learning	Understand

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	2	2				3	2	2
CO2	3	2	2				3	2	2
CO3	3	2	2				3	2	2
CO4	3						3		
CO5	3						3		

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Convolution:** Convolution Operation, Variants of the basic convolution function, Correlation, Filters, Feature Extraction, Pooling, Convolution and Pooling as an Infinitely Strong Prior, Structured Outputs, Random or Unsupervised Features. Convolutional Neural Networks, Relation between input size, output size and filter size, Visualizing filters of a CNN, Occlusion experiments, Finding influence of input pixels using backpropagation, Guided Backpropagation
Module 2	**Sequential Processing:** Sequential Processing: Sequence Learning, Recurrent Neural Networks, loss function, recurrent connections, teacher forcing training, Backpropagation through time (BPTT), Vanishing and Exploding Gradients, Truncated BPTT, Selective Read, Selective Write, Selective Forget - The Whiteboard Analogy, Long Short Term Memory, Gated Recurrent Units

Module 3	**Encoding Decoding:** Encoder Decoder Models, Applications of Encoder Decoder models, Attention Mechanism, Attention over images, Hierarchical Attention. Introduction to Autoencoders, Principal Component Analysis and Autoencoders, Regularization in autoencoders, Denoising and Sparse Signal processing, Denoising Autoencoders, Sparse Autoencoders, Contractive Autoencoders
Module 4	**Generation:** Generative Modeling, Principle of Generative Modeling, PixelRNN and PixelCNN, Variational Autoencoder, latent vector, reparameterisation trick, reconstruction and KL divergence loss, Generative Adversarial Network, Conditional Probability, Generator, Discriminator, Minimax objective function, gradient ascent, gradient descent
Module 5	**Strategies for Training and Regularisation:** Universal function approxination, Stochastic Gradient Descent, Momentum Based GD, Nesterov Accelerated GD, AdaGrad, RMSProp, Adam, Normalisation, Batch Normalization, Instance Normalization, Group Normalization. Regularization: Bias Variance Tradeoff, L2 regularization, Early stopping, Dataset augmentation, Parameter sharing and tying, Injecting noise at input, Adding Noise to the outputs, Early stopping, Ensemble Methods, Dropout

References:

[1] Heikki Huttunen, *Deep Neural Networks: A Signal Processing Perspective*, 3rd ed. Springer, 2019, pp. 133–163.

[2] Yu Hen Hu and Jenq-Neng Hwang, *Handbook Of Neural Network Signal Processing.* The Electrical Engineering And Applied Signal Processing Series, CRC Press, 2002.

[3] Christopher M. Bishop, *Pattern Recognition and Machine Learning.* Springer - Information Science and Statistics, 2011.

[4] Ian Goodfellow, Aaron Courville, and Yoshua Bengio, *Deep learning.* MIT press, 2016.

[5] Christopher M. Bishop, *Neural Networks for Pattern Recognition.* Oxford University Press, 1996.

25-509-0X20 **Image and Video Processing**

L	T	P	C
3	1	0	3

Prerequisites : Calculus and Matrices
Course Description : This course deals with digital images and processing of digital images for various applications.
Course Outcome : After the completion of the course, the student will be able to

CO1	Use basic image processing algorithms in practical applications	Apply
CO2	Select a suitable transform for the analysis of images	Analyze
CO3	Model image restoration/degradation	Apply
CO4	Apply image representation schemes for various applications	Apply
CO5	Demonstrate various video modeling techniques	Apply

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	2	3	2			2	3	
CO2	3	2	3	2				3	2
CO3	3	3	3					3	2
CO4	3	2	2					3	2
CO5	3	2	2				2	3	

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Fundamentals of Image Processing:** 2D systems & mathematical preliminaries - Linear systems and shift invariance, Fourier transform, optical and modulation transfer functions, matrix notation, Toeplitz and Circulant matrices, orthogonal and unitary matrices, block matrices and kronecker products, Types of images – black & white, gray scale and color images, basic relationship between pixels, intensity transformations and spatial filtering, filtering in frequency domain
Module 2	**Image Transforms:** Two-dimensional orthogonal and unitary transforms, separable unitary transforms, basis images, Kronecker products and dimensionality, properties of unitary transformations, dimensionality of image transforms, two dimensional DFT, cosine transform, sine transform, Hadamard transform, Haar transform, the KL transform

Module 3	**Image Restoration and Reconstruction:** A model of image degradation/restoration process, noise models, restoration in the presence of noise only using spatial filtering, periodic noise reduction using frequency domain filtering, linear position invariant degradations, estimating the degradation function, inverse function, wiener filtering, image reconstruction from projections
Module 4	**Morphology, Segmentation and Representation:** Morphological operations - dilation, erosion, opening and closing, Image segmentation - point, line and edge detection, thresholding, region growing, region splitting and merging, boundary preprocessing - chain codes, boundary approximation using minimum perimeter polygons, signatures, boundary feature descriptors - shape numbers, Fourier descriptors, statistical moments, region feature descriptors - compactness, circularity, eccentricity, topological descriptors - Euler number, texture descriptor based on histogram, graylevel co-occurrence matrix
Module 5	**Video Processing:** Video formation, perception and representation - principles of color video imaging, video cameras, video display, composite versus component video, gamma correction, analog video raster - progressive and interlaced scans, characterization of a video raster, video modeling -camera model, illumination model, object models, scene models, 2D motion models, 2D motion estimation - optical flow, pixel based motion estimation

References:

[1] Rafael C. Gonzalez and Richard E. Woods, *Digital Image Processing*, 4th ed. Pearson, 2018.

[2] Anil K. Jain, *Fundamentals of Digital Image Processing*, 1st ed. Pearson, 2015.

[3] Yao Wang, Jörn Ostermann, and Ya-Qin Zhang, *Video Processing and Communications*, 1st ed. Prentice Hall Upper Saddle River, NJ, 2002.

[4] Bhabatosh Chanda and Dwijesh Dutta Majumder, *Digital Image Processing and Analysis*, 1st ed. PHI Learning Pvt. Ltd., 2011.

[5] Subramania Jayaraman, S. Esakkirajan, and T. Veerakumar, *Digital Image Processing*, 2nd ed. Tata McGraw Hill, 2020.

[6] Alan C. Bovik, *Handbook of Image and Video Processing*. Academic press, 2010.

[7] Kenneth R. Castleman, *Digital Image Processing*, 1st ed. Pearson, 2007.

[8] Bernd Jähne, *Digital Image Processing*, 6th ed. Springer, 2005.

[9] William K. Pratt, *Digital Image Processing: PIKS Scientific Inside*, 4th ed. Wiley Online Library, 2007.

[10] Wayne Niblack, *An Introduction to Digital Image Processing*. Strandberg Publishing Company, 1985.

25-509-0X21 **Advanced Digital Signal Processing**

L	T	P	C
3	1	0	3

Prerequisites : Signals & Systems, Digital Signal Processing, Mathematics
Course Description : This course deals with the analysis & design of analog and digital DSP filters.
Course Outcome : After the completion of the course, the student will be able to

CO1	Determine the discrete Fourier transform of a signal	Apply
CO2	Select a suitable digital filter based on the application	Analyze
CO3	Illustrate multidmensional signals	Apply
CO4	Model multirate digital systems	Apply
CO5	Demonstrate DSP real world problems in hardware	Apply

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	2	2				3	2	
CO2	3	3	2					2	3
CO3	3	2	2				3	2	
CO4	3	3	2				3	2	
CO5	3	2	2					2	3

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Discrete-time Signals and Systems:** Discrete-time signals, systems, analysis of discrete-time linear time invariant system, discrete-time system described by difference equation, correlation of discrete-time signals, z-transform, analysis of linear time invariant system in z-domain, linear time invariant systems as frequency-selective filters, Discrete Fourier Transform (DFT) and its properties, implementation of discrete-time systems
Module 2	**Digital Filters:** Design of Finite Impulse Response (FIR) filters - symmetric and antisymmetric FIR filters, design of linear-phase FIR filters using windows, design of linear-phase FIR filters by the frequency-sampling method, design of FIR differenti ators, design of Hilbert transformers, design of Infinite Impulse Response (IIR) filters - design by approximation of derivatives, impulse invariant technique, bilinear transformation, frequency transformations

Module 3	**Multidimensional Signal Processing:** Two dimensional discrete signals, multidimensional systems, Linear Shift Invariant (LSI) systems, separable systems, stable systems, regions of support, vector input-output systems, frequency response of 2D LSI systems, multidimensional Fourier transform, properties od 2D Fourier transform, periodic sampling with rectangular geometry, multidimensional discrete Fourier series and transform, multidimensional z-transforms
Module 4	**Multirate Signal Processing:** Basic multirate operations - decimation and interpolation, aliasing, decimation filters and interpolation filters, fractional sampling rate alteration, digital filter banks - DFT filter banks, uniform DFT banks, time-domain descriptions of multirate filters, interconnection of building blocks, Noble identities, the polyphase representation, efficient structures for decimation and interpolation filters, polyphase implementation
Module 5	**DSP Processors:** Features of DSP processors, Von Neumann architecture vs Harvard architecture, Very Long Instruction Word (VLIW) architecture, TMS320C6x Architecture, Functional units, Linear and circular addressing modes, TMS320C6x instruction set, OMAP-L138 development system - C6748 processor, code composer studio IDE, support files, TLV320AIC3106 (AIC3106) onboard stereo codec for analog input an output, real-time input and output using polling, interrupts, and direct memory access, real time sine wave generation

References:

[1] John G. Proakis and Dimitris G. Manolakis, *Digital Signal Processing: Principles, Algorithms, and Application*, 4th ed. Pearson Education India, 2007.

[2] Rulph Chassaing, *Digital Signal Processing and Applications with the C6713 and C6416 DSK*, 1st ed. John Wiley & Sons, 2005.

[3] Donald S. Reay, *Digital Signal Processing and Applications with the OMAP-L138 eXperimenter*, 1st ed. John Wiley & Sons, 2012.

[4] Parishwad P. Vaidyanathan, *Multirate Systems and Filter Banks*, 1st ed. Pearson Education India, 2006.

[5] Dan E. Dudgeon and Russell M. Merserau, *Multidimensional Digital Signal Processing*, 1st ed. Prentice Hall, 1984.

[6] Sanjit K. Mitra, *Digital Signal Processing: A Computer-Based Approach.* McGraw-Hill Higher Education, 2001.

[7] Alan V. Oppenheim and Ronald W. Schafer, *Discrete-time Signal Processing*, 2nd ed. Prentice Hall, 1999.

[8] Chi Tsong Chen, *Digital Signal Processing: Spectral Computation and Filter Design.* Oxford University Press, Inc., 2001.

[9] Emmanuel C. Ifeachor and Barrie W. Jervis, *Digital Signal Processing: A Practical Approach.* Pearson Education, 2004.

25-509-0X22 **Real Time Operating Systems**

L	T	P	C
3	1	0	3

Prerequisites : Programming basics
Course Description : This course provides an understanding on the various aspects of real time operating systems. It covers methodologies in task scheduling and resource management.
Course Outcome : After the completion of the course, student will be able to

CO1	Solving shared data problems using multi-threaded programming	Apply
CO2	Understand OS architecture basics and RTOS approaches	Understand
CO3	Identify feasible schedules using various scheduling algorithms	Analyze
CO4	Discuss resource management and deadlock avoidance techniques	Understand
CO5	Explain various commercial RTOS flavors including Free RTOS	Understand

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	3					3		
CO2	3						3		
CO3	3	3					3		
CO4	3						3		
CO5	3		2				3		

3-High; 2-Medium; 1-Low

Course Content:

Module 1	**Embedded system review:** CPU and memory types, Direct memory access, Interrupt basics, interrupt latency, disabling and masking interrupts **Shared data problems:** atomicity, critical section and its properties. Peterson's Solution, test and set, lock and swap **Multi-threaded programming:** SMT vs Co-operative threads, IEEE POSIX standard for programming, POSIX Threads, producer consumer example. POSIX primitives: Mutex, Condition variables, Semaphores
Module 2	**Operating systems:** UNIX System architecture, user mode and kernel mode, Application program Interface, system calls, Process Control Block, Process Scheduling, Context Switch, Shared Memory, Message passing, Dining Philosopher's example **Software architectures & RTOS:** Embedded Architecture Types: Round Robin approach, Round-Robin with interrupts, Real Time Operating Systems. Soft and hard real time OS, tasks and task states, RTOS process life cycle, Reentrancy

Module 3	**Tasks scheduling:**Modeling of real time systems, Event triggered and Time triggered approach, Worst case execution time, pre-emptive priority systems, hybrid systems **Scheduling algorithms:** schedulability test and criteria, Fixed and dynamic priority scheduling – Rate Monotonic approach, First Come First Serve, Shortest Job First, Shortest Remaining Time, Earliest Deadline First, Gantt Charts. Time quantum, Multi-level queue, Little's formula
Module 4	**Communication and resource management:** Message queue, mailbox, pipes. Inter-task communication, Blocking and non-blocking task synchronization. Linear buffer, ring buffer, double buffering **Deadlock avoidance:** starvation, aging, resource allocation graph. Priority inversion, Nested critical sections, priority inheritance, disadvantages, priority ceiling protocol
Module 5	**RTOS software development:** Host and target machines, cross compilers, Linker, locator, emulators. Review of free and commercial Real Time Operating Systems- VxWorks, RTlinux, uCOS, etc. **FreeRTOS:** architecture and simulation on embedded platforms. RTOS Programming practise in FreeRTOS

References:

[1] David E. Simon, *An Embedded Software Primer*. Pearson Education, 2000.

[2] Abraham Silberschatz, *Operating Systems Concepts*. John Wiley & Sons, 20004.

[3] Herman Kopetz, *Real-Time systems, Design principles for distributed embedded applications*. Springer, 2011.

[4] Philip A. Laplante, *Real- Time Systems Design and Analysis*. John Wiley & Sons, 2004.

[5] Frank Vahid and Tony Givargis, *Embedded System Design: A Unified Hardware/ Software Introduction*. John Wiley & Sons, 1999.

[6] Wayne Wolf, *, Computers as Components: Principles of Embedded Computing System Design*. Elsevier, 2000.

[7] VxWorks, "https://www.windriver.com/products/vxworks/."

[8] Micrium μC/OS, "https://www.micrium.com/rtos/kernels/."

[9] Real Time Linux, "https://wiki.linuxfoundation.org/realtime/start/."

[10] Nicolas Melot, "Study of an Operating System: FreeRTOS," *CAPÍTULO XVIII*, vol. 115, pp. 1–39, 2009.

25-509-0X23 **Image & Video Processing Lab**

L	T	P	C
0	0	4	2

Prerequisites : Signals & Systems, Image Processing
Lab Description : This lab involves implementation of basic image and video processing techniques in Octave/MATLAB/Python.
Course Outcome : After the completion of the lab, the student will be able to

CO1	Use basic image processing toolbox in Octave/MATLAB/Python	Apply
CO2	Apply basic image processing operations	Apply
CO3	Select necessary 2D transform based on application	Analyze
CO4	Illustrate the importance of high frequency components in an image	Analyse
CO5	Outline the steps involved in video processing	Analyse

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1			3	3	2	2	2	2	3
CO2			3	3	2	2	2	2	3
CO3			3	3	2	2	2	2	3
CO4			3	3	2	2	2	2	3
CO5			3	3	2	2	2	2	3

3-High; 2-Medium; 1-Low

Course Content:

Sample List of Experiments*	
1	Introduction to image processing toolbox
2	Implementation of 2D convolution and 2D DFT
3	Point operations & histogram Processing
4	To perform histogram equalisation
5	Implementation of smoothing filters
6	Perform Image Sharpening & Edge Detection
7	Implement frequency domain filtering
8	Compute 2D DCT and KL transform
9	Implement image segmentation algorithms
10	Compute motion estimation of videos

* The list is not exhaustive. Additional experiments or project based on the experiments can be included in the laboratory activity.

References:

[1] Rafael C. Gonzalez and Richard E. Woods, *Digital Image Processing*, 4th ed. Pearson, 2018.

[2] Subramania Jayaraman, S. Esakkirajan, and T. Veerakumar, *Digital Image Processing*, 2nd ed. Tata McGraw Hill, 2020.

[3] Anil K. Jain, *Fundamentals of Digital Image Processing*, 1st ed. Pearson, 2015.

[4] Alasdair McAndrew, *An Introduction to Digital Image Processing with MATLAB*, 1st ed. Course Technology Press, 2004.

25-509-0X24 **Robotics Lab**

L	T	P	C
0	0	4	2

Prerequisites : None
Lab Description : This lab includes experiments using SCARA robot, Raspberry pi and Jetson Nano-supported robots, Robot Operating System(ROS) and Robotics toolbox from MATLAB.
Course Outcome : After the completion of the lab, the student will be able to

CO1	Program SCARA robot to perform tasks	Understand
CO2	Integrate and use ROS packages for various robotic applications	Apply
CO3	Demonstrate the robot‘s capability for autonomous mapping and localization	Apply
CO4	Navigate the robot through a cluttered environment without colliding with obstacles	Apply
CO5	Develop an optimized and efficient path that shows the intelligent navigation capability of the robot	Analyze

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	3	3	3	3	3	3		3
CO2	3	3	3	3	3	3	3	3	3
CO3	3	3	3	3	3	3	3		3
CO4	3	3	3	3	3	3	3	3	3
CO5	3	3	3	3	3	3	3	3	3

3-High; 2-Medium; 1-Low

Course Content:

Sample List of Experiments*	
1	Program the SCARA robot for transfer of objects from one position to another
2	Learn and implement various ROS packages
3	Implement SLAM algorithms to enable the robots to map an unknown environment while simultaneously localizing themselves to that environment
4	Develop an obstacle avoidance algorithm that allows the robot to navigate around obstacles in its path
5	Experiment with different path planning algorithms and find the most efficient route from one point to another

* The list is not exhaustive. Additional experiments or project based on the experiments can be included in the laboratory activity.

References:

[1] Morgan Quigley, Brian Gerkey, and William D. Smart, *Programming Robots with ROS: A Practical Introduction to the Robot Operating System.* O'Reilly Media, 2015.

[2] Lentin Joseph, *Mastering ROS for Robotics Programming.* Packt, 2015.

[3] Carol Fairchild and Thomas L. Harman, *ROS Robotics By Example.* Packt, 2017.

[4] Roland Siegwart, Illah Reza Nourbakhsh, and Davide Scaramuzza, *Introduction to Autonomous Mobile Robots.* MIT Press, USA, 2011.

[5] Mobile Robtics resources from MATLAB , "https://in.mathworks.com/solutions/robotics /resources.html."

25-509-0X25 **Semiconductor Device Modeling Lab**

L	T	P	C
0	0	4	2

Prerequisites : Taken with Device Physics And Modeling for Integrated Circuits
Lab Description : This lab prepares students to use TCAD device simulation software for semiconductor device simulation, modeling and parameter extraction.
Course Outcome : After the completion of the lab, the student will be able to

CO1	Use TCAD software for device characterization, modeling and simulation	Apply
CO2	Extract PN junction and MOSFET device parameters from characteristics	Apply
CO3	Use extracted MOSFET device parameters in ciruit simualtion models	Apply

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3		3	2	2	2	3		3
CO2	3		3	2	2	2	3		3
CO3	3		3	2	2	2	3		3

3-High; 2-Medium; 1-Low

Course Content:

Sample List of Experiments*	
1	Familiarization of TCAD software
2	PN junction I-V characteristics and parameter extraction
3	Study the effect of doping concentration on device characteristics
4	Model long channel MOSFETS, vary dimensions and doping and study how channel length modulation, body effect and subthreshold conduction affect device characteristics
5	Model MOSFETs at various gate lengths, study how short and narrow channel effects impact device performance
6	Extract MOSFET parameters from device characteristics, use the parameters in circuit simulation models
7	Model FINFETs and study the characteristics

* The list is not exhaustive. Additional experiments or project based on the experiments can be included in the laboratory activity.

References:

[1] Theodore I. Kamins and Richard S. Muller, *Device Electronics for Integrated Circuits*, 3rd ed. Wiley, 2002.

[2] Sentaurus TCAD Documentation from Synopsys Inc. , "https://www.synopsys.com/manufacturing/tcad/device-simulation/sentaurus-device.html."

25-509-0X26 **Processor Architecture Lab**

L	T	P	C
0	0	4	2

Prerequisites : Taken with 25-509-0X18, basic programming

Lab Description : The lab will include design and simulation of a simple RISC-V processor core. The lab will also provide a hands-on experience on simulator for evaluating the performance of various processor configurations.

Course Outcome : After the completion of the lab, the student will be able to

CO1	Design basic buiding blocks for the design of a RISC-V processor pipeline	Analyze
CO2	Design RISC-V processors with performance optimization and hazard avoidance techniques	Analyze
CO3	Compare the performance of various processor configurations in a processor simulator using benchmarks	Evaluate

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	3	3	3	3	3	3	3	3
CO2	3	3	3	3	3	3	3	3	3
CO3	3	3	3	3	3	3	3	3	3

3-High; 2-Medium; 1-Low

Course Content:

Sample List of Experiments*	
1	Design the components required for simple data path for RISC-V architecture in Verilog/BSV
2	Design the control path for for simple single cycle implementation of RISC-V architecture in Verilog/BSV
3	Design a simple pipelined RISC-V processor in Verilog/BSV
4	Implement a unicore system in processor simulator for a given memory hierarchy specification
5	Implement cache block replacement policy and analyse various parameters.
6	Build an ISA and for given specification, analyse performance parameters (like overall CPI, number of simulated CPU cycles, instruction issue rate, etc.)
7	Performance analysis of a given configuration for various benchmarks

* The list is not exhaustive. Additional experiments or project based on the experiments can be included in the laboratory activity.

References:

[1] John L. Hennessy and David A. Patterson, *Computer Architecture - A Quantitative Approach.* Morgan Kaufmann, 2017.

[2] David A. Patterson and John L. Hennessy, *Computer Organization and Design,The Hardware/Software interface: RISC-V Edition* . Morgan Kaufman, 2017.

[3] William Stallings, *Computer Organization and Architecture.* Pearson Ed, 2022.

[4] Arvind, Rishiyur S. Nikhil, James C. Hoe, and Silvina Hanono Wachman, "Introduction to digital design as cooperating sequential machines."

[5] "RISC-V International," https://riscv.org/.

[6] "Bluespec Reference Guide," https://web.ece.ucsb.edu/its/bluespec/doc/BSV/reference-guide.pdf.

[7] J. Bhasker, *A Verilog HDL Primer.* Star Galaxy Publishing, 2005.

[8] Shakthi Processors, " https://shakti.org.in/."

[9] Vega Processors, "https://vegaprocessors.in/."

[10] gem5 Simulator, "https://www.gem5.org/."

25-509-0X27 Deep Neural Network Signal Processing Lab

L	T	P	C
0	0	4	2

Prerequisites : Neural Networks
Lab Description : This lab provides experiments to implement deep neural network architectures and algorithms for spatial and temporal signal processing using Python with the help of open source libraries such as TensorFlow, Keras, PyTorch etc.
Course Outcome : After the completion of the lab, the student will be able to

CO1	Model CNN for feature extraction and predictions	Apply
CO2	Model RNN for temporal and sequential signals	Apply
CO3	Model encoder-decoder based neural networks for spatial/temporal signals	Apply
CO4	Model generative networks to generate signals/images	Apply
CO5	Propose DNN solution for real world problems and analyse models/algorithms for performance improvement	Analyse

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1			3	3	2	2	3	2	3
CO2			3	3	2	2	3	2	3
CO3			3	3	2	2	3	2	3
CO4			3	3	2	2	3	2	3
CO5			3	3	2	2	3	3	3

3-High; 2-Medium; 1-Low

Course Content:

Sample List of Experiments*	
1	Implement CNN, analyse the feature extraction, visualise the feature vectors using images
2	Implement RNN using LSTM/GRU to predict sequence/temporal signal
3	Implement encoder-decoder models for sequence/spatial signal
4	Implement generative adversarial network for signals/image generation
5	Solution proposal for a real world problem, model a deep neural network utilising CNN/RNN/encoder-decoder/GAN networks or ensemble models and analyse and evaluate the performance of model. Analyse better optimisation methods, regularisation aspects, data augmentation, etc. and improve the performance of model

* The list is not exhaustive. Additional experiments or project based on the experiments can be included in the laboratory activity.

References:

[1] Jon Krohn, *Deep Learning with TensorFlow, Keras, and PyTorch*. Pearson, 2020.

[2] Aurélien Géron, *Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow*, 3rd ed. O'Reilly Media, Inc., 2022.

[3] Documentations of python libraries.

25-509-0X28 **FPGA System Design Lab**

L	T	P	C
0	0	4	2

Prerequisites : Digital design basics
Lab Description : This lab equips students to build embedded systems using FPGA SOCs.
Course Outcome : After the completion of the lab, the student will be able to

CO1	Compare resource utilization, area and power for different implementations of digital logic blocks on FPGA	Evaluate
CO2	Demonstrate the functionality of different FPGA I/O interfaces	Apply
CO3	Integrate processor cores, memory and arithmetic blocks, transceivers and programmable logic in FPGA for practical applications	Evaluate

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	3	3	2	2	2	3		3
CO2	3	3	3	2	2	2	3		3
CO3	3	3	3	2	2	2	3	2	3

3-High; 2-Medium; 1-Low

Course Content:

Sample List of Experiments*	
1	Familiarization of Xilinx Vivado software
2	Implement basic logic blocks like adders, counters, shift registers on FPGA
3	Implement different types of multipliers and compare speed and resource utilization
4	Write a C program and run it on a single processor system, based on a MicroBlaze soft core, using the available Xilinx FPGA platform
5	Implement AXI-Lite peripheral with a Cortex-A9 Processing System on FPGA and demonstrate using GPIOs
6	Demonstrate a functional HDMI output system using Cortex-A9 Processing System on FPGA
7	Boot any OS on Cortex-A9 Processing System on FPGA

* The list is not exhaustive. Additional experiments or project based on the experiments can be included in the laboratory activity.

References:

[1] Ron Sass and Andrew G. Schmidt, *Embedded Systems Design with Platform FPGAs, Principles and Practices*. Elsevier, 2007.

[2] Matlab Resources: Digital system design and FPGA system design , "https://content.mathworks.com/viewer/642a7100f19355331a3ea4c2."

[3] Xilinx FPGA user guides and documentation.

[4] Xilinx Vivado documentation.

[5] ARM Advanced System on Chip Design Education Kit.

25-509-0X29 **Analog IC Design Lab**

L	T	P	C
0	0	4	2

Prerequisites : Taken with Analog IC Design
Lab Description : This lab explores the different stages of custom IC design flow using EDA tools and employs these steps for implementing analog circuit components.
Course Outcome : After the completion of the lab, the student will be able to

CO1	Simulate analog circuit components and estimate parameters like gain, bandwidth, power dissipation, noise figure etc.	Apply
CO2	Complete physically verified layouts from schematics for custom designs	Apply
CO3	Compare different implementations of analog integrated circuit components	Analyze

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3		3	2	2	2	3		3
CO2	3		3	2	2	2	3		3
CO3	3		3	2	2	2	3	2	3

3-High; 2-Medium; 1-Low

Course Content:

Sample List of Experiments*	
1	Cadence Spcetre circuit simulator familiarization
2	Learn the various steps of layout design like DRC, LVS and parasitic extraction using Cadence Virtouso layout editor
3	MOSFET characterization and parameter extraction
4	Design, simulate and compare various current mirror circuits
5	Design and simulate various inverting amplifier configurations
6	Design and simulate various differential amplifiers
7	Simulate operational transconductance amplifiers
8	Monte Carlo analysis

* The list is not exhaustive. Additional experiments or project based on the experiments can be included in the laboratory activity.

References:

[1] Behzad Razavi, *Design of Analog CMOS Integrated Circuit*, 2nd ed. McGraw Hill India, 2017.

[2] Documentation for Cadence Virtuoso custom IC simulation and layout suite.

25-509-0X30 **Neural Networks Lab**

L	T	P	C
0	0	4	2

Prerequisites : None
Lab Description : This lab provides experiments to implement neural network algorithms using Python with the help of open source libraries such as TensorFlow, Keras, PyTorch, etc.
Course Outcome : After the completion of the lab, the student will be able to

CO1	Implement regression models using neural network	Apply
CO2	Implement classifier models using a neural network	Apply
CO3	Solving non-linear problems using multi-layer neural network	Apply
CO4	Solution proposal for a real world problem	Apply
CO5	Analyse the models and improve the learning algorithms through parameter tuning	Analyse

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1			3	3	2	2	3	2	3
CO2			3	3	2	2	3	2	3
CO3			3	3	2	2	3	2	3
CO4			3	3	2	2	3	2	3
CO5			3	3	2	2	3	3	3

3-High; 2-Medium; 1-Low

Course Content:

Sample List of Experiments*	
1	Familiarisation of Python, Jupyter notebook and libraries like TensorFlow, Keras, PyTorch, etc.
2	Implement the Perceptron model with gradient descent optimisation
3	Model a multilayer feed forward neural network and implement back propagation algorithm
4	Model neural networks for Regression tasks and Classification tasks for linear and non-linear data
5	Improve neural network model by fine tuning hyper-parameters, improve learning using heuristics and analyse training, validation and testing results
6	Solution proposal for a real world problem, model a neural network, pre-process the data, train the model and evaluate the performance and improve the learning through parameter tuning

* The list is not exhaustive. Additional experiments or project based on the experiments can be included in the laboratory activity.

References:

[1] Aurélien Géron, *Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow, 3rd Edition.* O'Reilly Media, Inc., 2022.

[2] Jon Krohn, *Deep Learning with TensorFlow, Keras, and PyTorch.* Pearson, 2020.

[3] Documentations of python libraries.

25-509-0X31 **Real Time Operating Systems Lab**

L	T	P	C
0	0	4	2

Prerequisites : Embedded Systems Lab
Lab Description : This lab will involve working on software tools and programming software for real time systems.
Course Outcome : After the completion of the lab, the student will be able to

CO1	Familiarize with parallel programming primitives and deadlock situations	Analyze
CO2	Implement thread safe programs for parallel threaded environments	Apply
CO3	Illustrate porting an open source RTOS into development boards for demonstrating real world scenarios	Apply
CO4	Customize operation of an RTOS to desired specifications	Apply

COs to POs and PSOs Mapping:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3		3	2	2	2	3		
CO2	3	2	3	2	2	2	3		
CO3	3	2	3	2	2	2	3	2	
CO4	3	2	3	2	2	2	3	2	

3-High; 2-Medium; 1-Low

Course Content:

Sample List of Experiments*	
1	Write a POSIX thread program with 25 threads generating a random number in them. The main thread should find the sum of all random numbers and the sum of all thread ids. Display these sums and end the child threads safely
2	Write a POSIX program to design a producer consumer example with buffer of size 10 between them. There should be checks in place using semaphores to avoid writing to full buffer and to prevent reading from empty buffer
3	Port FreeRTOS into Arudino board and write a program to blink LED for a fixed duration
4	Port FreeRTOS into XILINX Zybo board containing ARM processor using VIVADO. Flash sample program to blink LEF for a fixed duration
5	Demonstrate multi-level queue scheduling with pre-emption in FreeRTOS using a custom program
6	Implement Earliest Deadline First scheduling in FreeRTOS and display the schedule taken based on varying execution times and deadlines for tasks from user

* The list is not exhaustive. Additional experiments or project based on the experiments can be included in the laboratory activity.

References:

[1] David E. Simon, *An Embedded Software Primer*. Pearson Education, 2000.

[2] Abraham Silberschatz, *Operating Systems Concepts*. John Wiley & Sons, 20004.

[3] Herman Kopetz, *Real-Time systems, Design principles for distributed embedded applications*. Springer, 2011.

[4] Philip A. Laplante, *Real- Time Systems Design and Analysis*. John Wiley & Sons, 2004.

[5] Frank Vahid and Tony Givargis, *Embedded System Design: A Unified Hardware/ Software Introduction*. John Wiley & Sons, 1999.

[6] Wayne Wolf, *, Computers as Components: Principles of Embedded Computing System Design*. Elsevier, 2000.

[7] VxWorks, "https://www.windriver.com/products/vxworks/."

[8] Micrium μC/OS, "https://www.micrium.com/rtos/kernels/."

[9] Real Time Linux, "https://wiki.linuxfoundation.org/realtime/start/."

[10] Nicolas Melot, "Study of an Operating System: FreeRTOS," *CAPÍTULO XVIII*, vol. 115, pp. 1–39, 2009.