Curriculum Vitae of Dr. Tripti S Warrier

1. Name : **Dr. Tripti S Warrier**

2. Address : "Maitri ", Opp. Sanskrit College,
Tripunithara – 682301.

3. Date of Birth : 26/08/1980

4. Academic Qualifications:

Degree	University	Year of passing	Subjects/ Specialization	Class
PhD	IITM	2016	Computer Architecture	Distinction
MTECH	MANIPAL UNIVERSITY	2005	Digital Electronics & Communication	Distinction
BTECH	CUSAT	2002	Electronics	Distinction

5. Organizational Positions Held

- IEEE Member
- ACM SIGARCH Member

6. Professional Experience:

Designation	Institution	Period
Associate Professor	Muthoot Institute of Technology and Science, Varikoli	January'17-March'18
Associate Professor	Adi Shankara Institute of Science and Technology, Kalady	February'16-January'17
Senior Research Fellow	RISE Lab, Indian Institute of Technology Madras	December'08-December'09
Senior Project Engineer	Wipro Technologies	September'06-August'08
Senior Research Fellow	Naval Physical and Oceanographic Laboratory, Cochin	August'06-September'06

7. Scholarships

- MHRD scholarship for a period of 3 years (2012 – 2015) during PhD at IITM.

8. Fields of Research and Teaching:

- Computer Architecture - Multi-core Systems
- Memory Systems
- VLSI Design
- Microprocessor and Embedded Design

9. Projects Undertaken:

10. Professional Training Experience:

Undergone the following Refresher courses:

Sl. No.	Title	Institution	Duration
1	Hands-on Workshop on IoT and Embedded System Design	Muthoot Institute of Technology and Science	19th -23rd July 2017
2	System Design Using Vivado Design Suite and Zynq-7000 SoC Kit	Muthoot Institute of Technology and Science	21st - 22nd March 2017
3	Embedded System Design using ARM processor	Adishankara Institute of Engineering and Technology	15th July 2016

11. Conferences & Workshops Attended:

- 24th IEEE International Conference on High Performance Computing, Data, and Analytics, held at Jaipur, from 18th to 21st December 2017.
- 21st International Conference on Parallel Architectures and Compilation Techniques, held at Minneapolis, from 19th to 23rd September 2012.
- IEEE Computer Society Anual Symposium on VLSI, held at Indian Institute of Technology Madras, 4th to 6th July 2011.
- 24th IEEE International Conference on VLSI Design, held at Indian Institute of Technology Madras, 2nd to 7th January 2011.
- 16th IEEE International Conference on High Performance Computer Architecture, held at Indian Institute of Science, Bangalore, 9th to 14th January 2010.

12. Books Edited:

13. Technical Reports Brought Out:

14. Symposiums Organized:

- Workshop on Deep Learning for Computer Vision, Muthoot Institute of Technology and Science, Varikoli, 9th to 13th January 2018.
- "*Web Technologies* in an Industrial Perspective", Muthoot Institute of Technology and Science, Varikoli, 15th to 16th December 2017.
- *Workshop on Recent Trends in VLSI Technology*, Adishankara Institute of Technology and Science, Kalady, 3rd January to 7th January 2017.

15. Number of Students registered for Ph.D ***(Guide)*** **: 0**
(Co-Guide) **: 0**

16. Projects Guided:
M.Tech/ M.Sc **: 0**

17. Invited Talks Delivered

1. "Introduction to FPGA Programming using VIVADO", *Workshop on Recent Trends in VLSI Technology*, Adishankara Institute of Technology and Science, Kalady, 3rd January to 7th January 2017.
2. "Performance Optimization in Multicore systems using Cache Memory Management Techniques", *Faculty Development Programme On Advanced Computer Architecture,* College of Engineering Adoor, 19th December to 21st December 2016.
3. "Shared Cache Management in Multi-core Systems", Research Trends in Computing and Algorithms, in Government Model Engineering College, Thrikkakara from 25th to 29 th July 2016.
4. "Introduction to Multi-core Simulator: Gem5"*, Recent Trends in Computer Architecture*, in Rajagiri School of Engineering Technology, Kakkanad in November 2015.

18. Patents Filed

19. Awards

- Faculty travel grant to attend HiPC 2017.
- Student travel grant to attend PACT 2012.
- Outstanding Teaching Assistant Award at IITM 2012.
- Feather-in-my-cap award for DDR PHY project in Wipro Technologies (2006).

List of Publications

National Conferences

1. Tripti S Warrier, V P Felix. MVDR and STMV for Multiple Broadband Sources, Proceedings of SYMPOL 2005, CUSAT.

International Conferences

1. Raghavendra K, Tripti S Warrier, Madhu Mutyam, SAMO: Store Aware Memory Optimizations, ACM International Conference on Computing Frontiers, 2014, pp.33:1–33:10.
2. Tripti S Warrier, Anupama B, and Madhu Mutyam, An application-aware cache replacement policy for last-level caches, International Conference on Architecture of Computing (ARCS), Springer Lecture Notes on Computer Science (LNCS), 2013, pp. 207–219.
3. Raghavendra K, Tripti S Warrier, and Madhu Mutyam, SkipCache: Miss-rate Aware Cache Management. IEEE/ACM 2012 International Conference on Parallel Architectures and Compilation Techniques, PACT'12.
4. C.J. Janraj, T.V. Kalyan, Tripti Warrier, and Madhu Mutyam, Way sharing set associative cache architecture. IEEE International Conference on VLSI Design (VLSID'12), pp. 251-256, 2012.

Journals

International

1. Tripti S Warrier, Raghavendra K, Madhu Mutyam,"SkipCache : application aware cache management for chip multi processors", IET Computers & Digital Techniques, ISSN 1751-8601, doi:10.1049iet-cdt.2014.0150.