Dr. Bijoy Antony Jose

Assistant Professor
Department of Electronics
Cochin University of Science
and Technology

Curriculum Vitae

Experience

Industrial 6 years

Teaching 2 years

Projects Done

UG 2

PG 2

Ph. D. 2

Professional Training

Seminar 1

Workshops 3

FDPs 1

Conferences

Attended 5

Organised 4

Projects

PG Guidance 4

Consultancy 1

Awards & Achievements

Best Paper Award 2

Outstanding Graduate Student 1

Industry Award 4

Publications

International Journal 4

International Conference 10

Book Chapters 2

Teaching

Projects Done

Training Experience

Conferences

Projects

Achievements

Publications

Dr. Bijoy Antony Jose

Curriculum Vitae of Name of Faculty

1. Name : Dr. Bijoy Antony Jose

2. Address : 92 Vidya Nagar, Cochin University P.O.
Kochi 682022, Kerala

3. Date of Birth : 03-03-1983

4. Academic Qualifications:

Degree	University	Year of passing	Subjects/ Specialization	Class
B. Tech.	CUSAT	2004	Electronics & Comm.	First Class
M. S.	State University of New York	2006	VLSI design	First Rank/ GPA 3.97/4.0
Ph.D.	Virginia Tech.	2011	Embedded System/Software	GPA 3.9/4.0

5. Organizational Positions Held

- **IEEE member** since 2005
- **Program Chair** – Intl. Conf. on Advances in Computing and Communication, 2012, 2013, 2014.
- **Program Committee** – Intl. Conf. on Eco-friendly Computing and Communication Systems, 2012.

6. Professional Experience*:*

Designation	Institution	Period
Program Analyst Trainee	Cognizant Technology solutions India	Oct 2004- Jan 2005
Teaching Assistant	State University of New York	Jan 2005 – May 2006
System Programmer	IBM, New York, USA	Sep 2006- Nov 2006
Performance tools Software Engineer	Intel Corporation (Kelly Services), University of Illinois, USA	May 2008- Aug 2008
Software Engineer	Intel Corporation, Folsom, California, USA	May 2010 – Dec 2010
System-on- Chip Performance Engineer	Intel Corporation, Santa Clara, California, USA	Aug 2011- Aug 2014
Software Architect	Intel Mobile Communications, Bangalore India	Aug 2014 - Aug 2015
Assistant Professor	Department of Electronics, Cochin University of Science and Technology, India	Aug 2015 – current

7. Scholarships

- Graduate Teaching Assistantship – State University of New York
- Graduate Research Assistantship- Virginia Tech.

8. Fields of Research and Teaching:

Microprocessor and Embedded Systems, VLSI design, Operating Systems and Mobile computing.

9. Projects Undertaken:

Sl. No.	Title	Funding Agency	Amount	Duration
1.	Mobile Computing project	Agileblaze technologies	Rs. 47253	2 months
TOTAL OUTLAY GENERATED Rs. 47352				

10. Professional Training Experience:

Undergone the following Refresher courses:

Sl. No.	Title	Institution	Duration
1	Workshop on side channel based cyber threats and mitigation techniques	IIT Kanpur	Feb 8-11, 2016
2	IEEE APS Short term training Keysight ADS and EMPRo,	CUSAT DOE	Oct 28-30, 2015

11. Conferences & Workshops Attended:

IEEE Forum on specification and Design Languages, France 2008.
IEEE Design, Automation and Test in Europe, (DATE), France 2011.
Workshop on side channel based cyber threats and mitigation techniques, IIT Kanpur, 2016

12. Books Edited:

1. Bijoy A. Jose, Bin Xue, Sandeep K. Shukla and Jean-Pierre Talpin, "Programming models for Multi-Core Embedded Software," Book Chapter in: Multi-Core Embedded Systems, CRC Press, Taylor & Francis, April 2010. ISBN: 978-1-4398-1161-0.

2. Bijoy A. Jose and Sandeep K. Shukla, "MRICDF: A polychronous model for embedded software synthesis", Book Chapter: Synthesis of Embedded Software. Springer Circuits and Systems, 2010. ISBN: 978-1-4419-6399-4.

13. Technical Reports Brought Out:

Name	Nos.
Parallelizing MPEG encoder for Microsoft windows player on Intel Core machines was recommended and accepted to a weekly radio program about software developments happening worldwide. *http://software.intel.com/en-us/blogs/2010/10/26/parallel-programming-talk-95-bijoy-jose-multi-threading-for-higher-utilization-of-worker-threads-in-an-mpeg-encoder-halloween-show*	1
Bijoy A. Jose and Abhishek Agrawal, "Energy Efficiency of Virtual Machines," White paper at Intel Developer zone, 2011.	1

14. Symposiums Organized:

- **Program Chair** – Intl. Conf. on Advances in Computing and Communication, 2012, 2013, 2014.
- **Program Committee** – Intl. Conf. on Eco-friendly Computing and Communication Systems, 2012.

15. Number of Students registered for Ph.D ***(Guide)*** **: 0**
(Co-Guide) **: 0**

16. Projects Guided:
M.Tech/ M.Sc **:** 4 M. Sc. projects ongoing

17. Invited Talks Delivered

1. FDP resource person, Embedded Software for safety critical systems College of Engineering, Kidangoor.

18. Patents Filed

19. Awards

- **Outstanding Graduate Student –** Electrical Engineering Graduation Batch, SUNY New Paltz, 2006.
- **Best Paper Award**: 15th IEEE/ACM Asia South Pacific Design Automation Conference, Taiwan, 2010
- **Dissertation invited to Ph.D. Forum-** Design, Automation and Test in Europe (DATE), France, 2011, DATE is a highly rated conference which awards travel grants to Ph.D. students to present their work during Ph.D. Forum. Fewer than 50 students are selected from all over the world at the annual Ph.D. Forum.
- **Intel Group Recognition Award:** For Outstanding performance results obtained for Jellybean on Clover trail Tablet devices.
- **Intel Divisional Recognition Award:** For identifying a hardware issue in mobile computing device, Q4 2011.

- **Intel Divisional Recognition Award:** For fixing a loop snoop detection bug in mobile device, Q1 2012.
- **Intel Department Award:** For compiler optimizations to improve performance of Motorola Razr-i Android phone with Intel chip inside
- **Best paper award**: Primary author of a guide to identify and prototype optimizations in Android Dalvik VM at Intel. **"***A playbook for Analysis, Prototyping and Estimation of optimizations targeting Android Dalvik VM*" Intel Software Professional's Conference 2013.

List of Publications

International Conferences

1. Bijoy A. Jose, Abdoulaye Gamatie, Julien Ouy and Sandeep K. Shukla, SMT Based False Causal loop Detection during Code Synthesis from Polychronous Specifications, *ACM/IEE 9th Intl. Conf. on Formal Methods and Models for Codesign (MEMOCODE),* Cambridge, UK, July, 2011.

2. Bijoy A. Jose, Manuj Sabharwal and Abhishek Agrawal (Intel Corp. internship work), "Power implications of high resolution timer tick settings," *1st International Conference on Energy aware computing*, Egypt, Dec. 2010.

3. Bijoy A. Jose, Jason Pribble and Sandeep K. Shukla, "Faster software synthesis using Actor Elimination Techniques for Polychronous formalism," *in Proceedings of Applications of Concurrency to System Design (ACSD)*, Portugal, June 2010.

4. Bijoy A. Jose and Sandeep K. Shukla, An Alternative Polychronous Model and Synthesis Methodology for Model-Driven Embedded Software, *15th IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, Taiwan, Jan. 2010.

5. Mahesh Nanjundappa, Hiren D. Patel, Bijoy A. Jose and Sandeep K. Shukla, "SCGPSim: A Fast SystemC Simulator on GPUs," *15th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 149-154, Taiwan, Jan. 2010. [Best Paper Award]

6. Bijoy A. Jose, Jason Pribble, Lemaire Stewart, and Sandeep K. Shukla, "EmCodeSyn: A Visual Environment for Multi-Rate Data Flow Specifications and Code Synthesis for Embedded Applications," *12th Intl. IEEE Forum on specification and Design Languages (FDL'09)*, pp. 1-6, Sophia Antipolis, France, Sept. 2009.

7. Syed Suhaib, Bijoy A. Jose, Deepak A. Mathaikutty, and Sandeep K. Shukla, "Formal Transformation of a KPN specification into a GALS implementation," *Proc. of Forum on Specification and Design Languages (FDL'08)*, pp. 84-89, Germany, Sept. 2008.

8. Bijoy A. Jose, Sandeep K. Shukla, Hiren D. Patel, and Jean-Pierre Talpin, "On the Deterministic Multi-threaded Software Synthesis from Polychronous Specifications," *Proc. of the 6th ACM/IEEE International Conference on Formal Models and Methods in Co-Design (MEMOCODE'08)*, pp. 129-138, Anaheim, CA, June 2008.

9. Bijoy Jose and Damu Radhakrishnan, "Fast redundant binary partial product generators for Booth multiplication"," *Proc. of 50th IEEE Midwest Symposium on Circuits and Systems (MWSCAS'07)*, pp. 297-300, Montreal, Canada, Aug. 2007. [Best Paper Award finalist].

10. Bijoy Jose and Damu Radhakrishnan, "Delay Optimized Redundant Binary Adders," *Proc. of 13th IEEE International Conference on Electronics, Circuits and Systems (ICECS),* pp.514 - 517, Nice, France, Dec. 2006.

Journals

International

1. Bijoy Jose and Abhishek Agrawal, "Improving Energy efficiency of virtual machines with timer tick variations," 11(3), Journal of Low Power Electronics (JOLPE), 401-405, 2015.

2. Bijoy Jose and Damu Radhakrishnan, "Redundant binary partial product generators for compact accumulation in Booth multipliers," Elsevier Microelectronics Journal, 40(11), pp. 1606-1612, Nov. 200.

3. Bijoy A. Jose, Hiren D. Patel, Sandeep K. Shukla, Jean-Pierre Talpin, "Generating Multi-Threaded code from Polychronous Specifications," Electronic Notes on Theoretical Computer Science, 238:57-69, Jan. 2009.

4. Bijoy A. Jose, Bin Xue and Sandeep K. Shukla, An Analysis of the Composition of Synchronous Systems, Electronic Notes in Theoretical Computer Science, 245: 69-84, Aug., 2009.

Curriculum Vitae

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