Dr. BIJOY ANTONY JOSE

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EDUCATION

	Graduation
Doctor of Philosophy in Computer Engineering Virginia Polytechnic Institute and State University, USA.	August 2011
Master of Science in Electrical Engineering State University of New York at New Paltz, USA.	December 2006
Bachelor of Technology in Electronics and Comm. Engineering Cochin University of Science and Technology. India	May 2004

ACADEMIC WORK EXPERIENCE

	Joined	Duration
Assistant Professor at Department of Electronics Cochin University of Science and Technology, India	[2015]	[current]
Graduate Research Assistant FERMAT Lab, Virginia Tech, USA.	[2011]	[3 years]
Graduate Teaching Assistant State University of New York, New Paltz, USA.	[2006]	[1.5 years]

INDUSTRY WORK EXPERIENCE

Software Architect Intel Mobile Communications, Bangalore, India	[2014]	[1 year]
System on Chip Performance Engineer Intel Corporation, Santa Clara, California, USA.	**[**2011]	[3 years]
Program Analyst Cognizant Technology Solutions, India.	[2004]	[3 months]

INTERNSHIPS

Graduate Technical Intern Developer Relations Division Intel Corporation, Folsom, California, USA	[2010]	[7 months]
Performance Tools Software Engineer University of Illinois Corporate Research Park Intel Corporation, Champaign, Illinois, USA	[2008]	[3 months]
System Programmer Intern SystemZ benchmarking Team IBM Corporation, Poughkeepsie, New York, USA.	[2006]	[3 months]

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SUMMARY OF RESEARCH ACTIVITIES AT COCHIN UNIVERSITY

GRANTS

- **DST SERB Early Career Research Award:** Given to young faculty by Gov. of India. "Optimizations for Virtualized Mobile Computing" as sole Principal Investigator. Fund of Rs. **17.12 Lakhs**.

- **DST Interdisciplinary Cyber Physical Systems:** "Energy efficient cyber security implementations for Internet of Things" project in collaboration with IIT Patna and Qrio Technologies. Fund of **Rs. 25 Lakhs** approved in 2018.

- **IEEE Humanitarian Assistance Grant:** "Revival of flood affected Kerala School through technology" project awarded based on UN sustainable development goals for reviving flood affected Gov. School Kuttamassery, Aluva in 2019 for **Rs 24 Lakhs**

- **Erudite Scholar Grant from Kerala Higher Education Council:** Received support as co-ordinator (**Rs. 1,52,500/-**) to bring Prof. Dr. Narasimhan Sunderarajan from NTU Singapore for a Scholar in residence programme at Dept. of Electronics, CUSAT.

- **DST SERB International Travel Support:** Received travel and registration fee support **(Rs. 1,37,946/-)** from SERB to present paper at Columbia University, New York at the 4th IEEE Conference on Cyber Security and Cloud Computing.

- **CSIR Seminar Grant:** As co-ordinator got financial Support of **Rs 1,00,000** for 8th Intl. IEEE Symp. on Embedded Computing and System Design is being held at CUSAT on Dec 13-15.

- **KSCSTE Seminar Grant:** As co-ordinator got financial Support of **Rs 75,000** for 8th Intl. IEEE Symp. on Embedded Computing and System Design is being held at CUSAT on Dec 13-15.

CONSULTANCY

- **AI & Machine Learning:** Vuelogix Technologies: Rs 30,000/month from Jan 2020.
- **Mobile Computing Project:** Agileblaze Technologies, Kochi. Amount: Rs. 47352.
- **Pumex Infotech:** Monthly sum of Rs 20,000 from April 2018 to present. (Annual sum of Rs.2.4 Lakhs).
- **KITCO:** Consultant to Innovation cell dealing with Electronics and Information Technology starting November 2018.
- **Consulting fee:** 30 percent of all consulting fee is paid to Cochin University.

Honours At Academia

- **Early Career Research Award** – DST SERB research award for young faculty in India.
- **National Winner Embedded Security Challenge at CSAW 2018–** First prize for CPS lab members Bijoy, Akhil & Gisha at contest held at IIT Kanpur, beating security researchers

from IIT Kharaghpur, IIT Madras, IIT Kanpur, Amrita University and IIIT Allahabad in final round.

- **FLAIR Selection:** Selected by Higher Education department, Gov. of Kerala for Fostering Linkages in Academic Innovation and Research, 2016.
- **Young Scientist Conclave –** CSIR India International Science Festival presentation selection at NPL, New Delhi, 2016.
- **Atal Tinkering Lab Advisor:** Advisor to Atal Innovation Mission sponsored lab at TocH School for young students in 2018.
- **Outstanding Graduate Student –** Electrical Engineering Graduation Batch, SUNY New Paltz, 2006. Awarded to the best outgoing student of the graduation batch based on GPA and overall performance.
- **Dissertation invited to Ph.D. Forum-** Design, Automation and Test in Europe (DATE), France, 2011, DATE is a highly rated conference which awards travel grants to Ph.D. students to present their work during Ph.D. Forum. Fewer than 50 students are selected from all over the world at the annual Ph.D. Forum.
- **Graduation:** Highest GPA of graduating batch in Dept. for PhD (3.97) and Masters (3.9).
- **Best Paper Award:** *At the 7th International IEEE Conference on Smart Computing and Communication*, Curtin University, Malaysia, 2019.
- **Best Paper Award**: 15th IEEE/ACM Asia South Pacific Design Automation Conference, Taiwan, 2010. Our paper about simulating event driven systems using NVIDIA CUDA code on a GPU device was selected as the best paper for IEEE ASP-DAC conference in 2010.
- **Best Paper Award Finalist:** The 50th IEEE Midwest Symposium on Circuits & Systems, Canada, 2007.
- **Program Chair** – 8th IEEE Intl. Symp. On Embedded Computing and System Design, 2018.
- **Program Chair** – Intl. Conf. on Advances in Computing and Comunication, 2012. http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=06305536
- **Program Committee** – of several national and international conferences and workshops
- **Reviewer for major publications**: IEEE Transactions on computers, IEEE Design and Test magazine, IEEE Embedded Systems letters, IEEE Design and Test in Europe, ACM Transactions On Design automation of Electronic Systems.

Honours At Industry

- **Intel Group Recognition Award:** For Outstanding performance results obtained for Jellybean on Clover trail Tablet devices.
- **Intel Divisional Recognition Award:** For identifying a hardware issue in mobile computing device, Q4 2011.
- **Intel Divisional Recognition Award:** For fixing a loop snoop detection bug in mobile device, Q1 2012.
- **Intel Department Award:** For compiler optimizations to improve performance of Motorola Razr-i Android phone with Intel chip inside
- **Internship work at Intel featured in Parallel programming talk:** My work in parallelizing MPEG encoder for Microsoft windows player on Intel Core machines was recommended and accepted to a weekly radio program about software developments happening worldwide. *http://software.intel.com/en-us/blogs/2010/10/26/parallel-programming-talk-95-bijoy-jose-multi-threading-for-higher-utilization-of-worker-threads-in-an-mpeg-encoder-halloween-show*.
- **Best paper award :** Intel Software professional's Conference Santa Clara, 2013. **"***A playbook for Analysis, Prototyping and Estimation of optimizations targeting Android Dalvik VM*"

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SELECTED INVITED TALKS AND WORKSHOPS

- **Young Scientist Conclave Speaker:** An Indigenous Computer Aided Design tool for multifunction printers, 2nd India International Science Festival, CSIR, Dec. 2016.
- **Alumni talk at State University of New York:** Talk on Embedded Systems research areas at State University of New York at New Paltz, New York, USA, March 2016.
- **Program Chair of ISED:** 8th Intl. IEEE Symp. on Embedded Computing and System Design is being held at CUSAT on Dec 13-15. It was previously hosted by IIT Patna, NIT Suratkal, NIT Durgapur, NTU Singapore, etc.
- **Kochi Fights Air Pollution:** With Doctors org IMA, installed Pollution monitors and worked on creating awareness with District collector and Rotary organization.
- **Atal Tinkering Lab:** Inaugurated and advising Atal Tinkering lab at Toc-H school
- **Resource person at institutions:** College of Engineering Kidangoor, TocH engineering college, MES college, SoE CUSAT, Rajagiri engg college, NPOL, etc.
- **Session Chair and Program committee member:** ISED conf. at IIT Patna. 2016.
- **Attended sponsored workshops:** Workshop on Cyber Secruity at IIT Kanpur , IIT Patna, etc.

GUIDE FOR DOCTORAL STUDENTS

- **Deepa Mathew:** Working on Virtualization of Embedded Systems (2016 onwards)
- **Akhil P.:** Working on Cyber Security of Internet of Things (2016 onwards)
- **Gisha C. G.:** Working on hardware security implementations (2018 onwards)
- **Ajai J. C.:** Working on Machine learning for Video Surveillance (2019 onwards)

GRADUATE THESIS GUIDE

- **Nithin P. B.** Face Tracking Robot Testbed for Performance Assessment of Machine Learning Techniques, 2019
- **Grieshma Unnikrisnan.** Logistics improvement using IoT (With Intel) 2019.
- **Ruksin Kamal.** Machine Learning for Helmet identification (with KITCO) 2019.
- **Bustan Ahmed.** Emotion Recognition using Machine Learning Techniques, 2019
- **Vishupriya A. B.** High Performance computing using Tensorflow, 2018
- **Akhil P.** Stepper motor based graphics plotter with GUI. M. Tech., 2017.
- **Arya S.** A client server protocol with Intel Galileo. M. Sc. 2017
- **Keerthana M.** AES algorithm using GEZEL, 2016
- **Sreelakshmi M. S.** Wireless Sensor Network for temperature monitoring, 2016.
- **Internal guide**: for student projects at ITC Infotech and Qrio Technologies

MY ACADEMIC RESEARCH WORK

Ph.D. Dissertation: "Formal model driven software synthesis for embedded systems".
Advisor: Dr. Sandeep K. Shukla, Professor and IEEE Fellow, Virginia Tech, USA.

MRICDF formalism: A synchronous formalism (MRICDF) was proposed to model embedded software targeting safety critical systems such as drones, robots, sensors, etc. MRICDF is a data flow based modeling specification which can express various building blocks of control software. With these building blocks and a hierarchical model can be made for embedded software. We proved that a prime implicate generator can be used to find the synthesizable sequential designs which can be proved to be generating code that follow the specification.

EmCodeSyn: Built a software tool (EmCodeSyn) which generates C code from MRICDF specification. The tool can model, simulate and synthesize code for embedded systems. We interfaced SAT solvers, Model checkers to this tool to verify our claims are correct.

Collaborations: Funding for project EmCodeSyn is being continued from United States Air Force office of Scientific Research with additional PhD students and Post-Doctoral students joining the project. We have interacted with researchers from IRISA France, Univ. of Kaiserslautern and SUNY Albany who actively contributed to the project.

M.S. Thesis: "New Redundant Binary Adder Cells for Multiplier Design".
Advisor: Dr. Damu Radhakrishnan, Associate Prof., State University of New York at New Paltz, USA.

Designed delay optimized adders which work on redundant binary numbers. Proposed multiplier designs having better partial product generators using redundant binary arithmetic.

INDUSTRY WORK EXPERTISE

Embedded systems experience @ Intel Corporation

- **Low power smart devices in a virtualized environment**
  - Working as a software architect deciding platform specs to meet performance requirements in future mobile products.
  - Involved in meeting initial boot up and stability requirements of new products before handing over to product teams.
  - Working on Virtual Machines where application and communication processors are being shared (Intel SoFIA platform). Target is to achieve high LTE data rates without compromising on application performance.

- **Android Dalvik Virtual Machine Compiler Optimizations**
  - Part of Dalvik JIT compiler optimizations implemented in Intel Android for three years.
  - I implemented specific compiler optimizations for Android Dalvik JIT compiler.
  - Optimizations targeting general software quality for JIT, interpreter, Memory management were implemented.
  - Co-Author of the first patch and many more to support Dalvik on x86 devices in Android Open Source project maintained by Google.
    https://android-review.googlesource.com/#/c/38941/

- **Functional : Bring up, porting of android releases on Intel devices**
  - Bring up effort of android releases such as Ice cream sandwich and Jellybean on Intel mobile devices.
  - For Ice Cream Sandwich and Jellybean releases, bug triage and fixes for various aspects of Dalvik VM. These fixes covered both functional and performance features of Android mobile phones and Tablets.

- **Performance Analysis work on Mobile devices**
  - Worked on improving the performance of Dalvik VM calculated using key benchmarks such as Caffeinemark, Quadrant, Smartbench, etc.
  - Identified weaknesses in Intel's internal Android source contributing to lower scores in Key benchmarks. Provided patches to boost benchmark scores for various Android Intel devices.

- Primary author of a guide to identify and prototype optimizations in Android Dalvik VM at Intel. **"***A playbook for Analysis, Prototyping and Estimation of optimizations targeting Android Dalvik VM*" Intel Software Professional's Conference 2013 [Best Paper Award].

Building Software tools and enabling optimizations for processors

- **Intel Thread Checker tools**
  - At Performance Analysis and Threading I was involved in the test and development of a Intel Thread Checker tool feature which identifies multi-threading data conflicts in user code

- **Enabling SIMD operations for latest Intel processors**
  - Worked on performance enhancement of media codec and power analysis of software applications.
  - Multi-thread implementation of media codec and enabling Single Instruction Multiple Data instructions to speed up software applications.

- **Automated load testing for IBM SystemZ servers**
  - As a part of IBM SystemZ benchmarking Group, I automated the testing for efficiency in the distribution of work for mainframes.

MY ACADEMIC PROJECTS

1. Build EmCodeSyn tool which utilizes prime implicate generator, model checker & SAT solver to generate code and prove correctness [PhD, funded by National Science Foundation]
2. FPGA Spartan 3E implementation of computational blocks using HDL and C [PhD]
3. Multi-threaded code using CUDA on NVIDIA devices [PhD, funded by NVIDIA]
4. MATLAB implementation of a Dual Tone Multi-Frequency Encoder & Decoder [MS]
5. Layout and spice simulations of arithmetic blocks to evaluate power and performance [MS]
6. Software implementation of Programmable Interrupt Controller using VHDL [BTech]

SKILLSET

Software Tools: Visual Studio, GDB, VTUNE, Eclipse IDE, SAT solvers, Model Checkers.

Hardware Design Tools: Xilinx SDK, ModelSim, L-Edit, T- Spice.

Embedded Hardware Familiarity: FPGA Spartan 3E, Intel SoC, NVIDIA Tesla GPU, Microcontrollers 89C51, 8051.

Programming Familiarity: C, Android OS, SIGNAL (Dataflow), MATLAB, CUDA, GEZEL.

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PUBLICATION LIST

JOURNALS

- Nithin P.B, Albert Francis, Ajai John Chemmanam, Bijoy A Jose and Jimson Mathew, "Interactive Robotic Testbed for Performance Assessment of Machine Learning based Computer Vision Techniques," Journal of Information Science and Engineering, Vol. 36 No. 5, September, 2020 (impact factor 0.77)

- R. K. Sanodiya, Jimson Mathew, Biju Paul, and Bijoy A. Jose, "A Kernelized Unified Framework for Domain Adaptation," IEEE Access, vol. 7, pp. 181381-181395, 2019. (impact factor 4.96)

- Deepa Mathew, Bijoy A. Jose, and Priyadarsan Patra, "Performance Analysis of Microkernel Based Virtualization Techniques on Embedded Systems," Journal of Low Power Electronics (JOLPE), 15(2), pp. 273-281, June 2019. (impact factor 0.35)

- Jos Prakash, Babita Jose, Jimson Mathew, and Bijoy A. Jose, "A differential quantizer based error feedback modulator for analog to digital converters," IEEE Transactions on Circuits & Systems II, 99, pp. 1-5, Feb. 2017. (impact factor 3.52)

- Jos Prakash, Babita Jose, Jimson Mathew, and Bijoy A. Jose, "A triple-mode hexa-standard reconfigurable TI cross-coupled modulator," International Journal of Electronics, 104(7), pp. 1142-1160, Taylor & Francis, Mar. 2017. (impact factor 1.12)

- Bijoy Jose and Abhishek Agrawal, "Improving Energy efficiency of virtual machines with timer tick variations," Journal of Low Power Electronics (JOLPE), 11(3), 401-405, 2015. (impact factor 0.35)

- Bijoy Jose and Damu Radhakrishnan, "Redundant binary partial product generators for compact accumulation in Booth multipliers," Elsevier Microelectronics Journal, 40(11), pp. 1606-1612, Nov. 2009. (impact factor 1.57)

- Bijoy A. Jose, Hiren D. Patel, Sandeep K. Shukla, Jean-Pierre Talpin, "Generating Multi-Threaded code from Polychronous Specifications," Electronic Notes on Theoretical Computer Science, 238:57-69, Jan. 2009. (impact factor 0.79)

- Bijoy A. Jose, Bin Xue and Sandeep K. Shukla, An Analysis of the Composition of Synchronous Systems, Electronic Notes in Theoretical Computer Science, 245: 69-84, Aug., 2009. (impact factor 0.79)

BOOK CHAPTERS

- Bijoy A. Jose, Bin Xue, Sandeep K. Shukla and Jean-Pierre Talpin, "Programming models for Multi-Core Embedded Software," Book Chapter in: Multi-Core Embedded Systems, CRC Press, Taylor & Francis, April 2010. ISBN: 978-1-4398-1161-0.

- Bijoy A. Jose and Sandeep K. Shukla, "MRICDF: A polychronous model for embedded software synthesis", Book Chapter: Synthesis of Embedded Software. Springer Circuits and Systems, 2010. ISBN: 978-1-4419-6399-4.

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CONFERENCE PUBLICATIONS

- Deepa Mathew, Binish M. C., and Bijoy A. Jose, "Computationally Efficient Intra and Inter Mode Decision in H.264/AVC", Third International Conference on Computing and Network Communications (CoCoNet), Procedia Computer Science, Volume 171, 2020, Pages 360-368, 2020.

- Nithin P.B, Albert Francis, Ajai John Chemmanam, Bijoy A Jose, "Face Tracking Robot testbed for Performance Assessment of Machine Learning Techniques", *The 7th International IEEE Conference on Smart Computing and Communication*, Malaysia, June, 2019.

- Grieshma Unnikrishnan, Deepa Mathew, Bijoy A. Jose and Raju Arvind, "Hybrid Route Recommender System for Smarter Logistics", *The 4th IEEE International Conference on High Performance and Smart Computing (HPSC),* Washington DC, May 2019.

- Deepa Mathew and Bijoy A. Jose, "Performance Analysis of Virtualized Embedded Computing Systems", 7th *IEEE Intl. Symposium on Embedded computing and system Design (ISED)*, NIT Durgapur, Dec. 2017.

- Arya S, Deepa Mathew, Bijoy A. Jose, An Offline Online Strategy for IoT using MQTT, 4th IEEE International Conference on Cyber Security and Cloud Computing, New York, Columbia University, USA, June 2017.

- Ajai J. Chemmanam, Salmanul Faris K, Sreelekshmi. S., M.Vasu Sairam, and Bijoy A. Jose, Portable E-Voting decision system, 6th IEEE Intl. Conf. on Computer Comm. and Informatics (ICCCI), Coimbatore, Jan., 2017.

- Elizabeth George E., Elsa Mary Cyriac, Sreedevi K., and Bijoy A. Jose, Voice Biometric System Based Personnel Identification, *Kerala Technological Congress (KETCON-2017 Embedded systems and VLSI Technologies),* Kerala, Jan. 2017.

- Akhil P., Abhijith C. R. and Bijoy A. Jose, Interfacing a Computer Aided Design Tool with a Multi-Function Numerical Machine, *6th IEEE Intl. Symposium on Embedded computing and system Design (ISED),* IIT Patna, Dec. 2016.

- Akhil P., Abhijith C. R. and Bijoy A. Jose, An indigenous Computer Aided Design tool for multifunction printers, 2nd India International Science Festival, National Physical Laboratory, CSIR, New Delhi, Dec. 2016.

- Bijoy A. Jose, Abdoulaye Gamatie, Julien Ouy and Sandeep K. Shukla, SMT Based False Causal loop Detection during Code Synthesis from Polychronous Specifications, *ACM/IEEE 9th Intl. Conf. on Formal Methods and Models for Codesign (MEMOCODE),* Cambridge, UK, July, 2011.

- Bijoy A. Jose, Manuj Sabharwal and Abhishek Agrawal (Intel Corp. internship work), "Power implications of high resolution timer tick settings," *1st International Conference on Energy aware computing*, Egypt, Dec. 2010.

- Bijoy A. Jose, Jason Pribble and Sandeep K. Shukla, "Faster software synthesis using Actor Elimination Techniques for Polychronous formalism," *in Proceedings of Applications of Concurrency to System Design (ACSD)*, Portugal, June 2010.

- Bijoy A. Jose and Sandeep K. Shukla, An Alternative Polychronous Model and Synthesis Methodology for Model-Driven Embedded Software, *15th IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, Taiwan, Jan. 2010.

- Mahesh Nanjundappa, Hiren D. Patel, Bijoy A. Jose and Sandeep K. Shukla, "SCGPSim: A Fast SystemC Simulator on GPUs," *15th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 149-154, Taiwan, Jan. 2010. [Best Paper Award]

- Bijoy A. Jose, Jason Pribble, Lemaire Stewart, and Sandeep K. Shukla, "EmCodeSyn: A Visual Environment for Multi-Rate Data Flow Specifications and Code Synthesis for Embedded Applications," *12th Intl. IEEE Forum on specification and Design Languages (FDL'09)*, pp. 1-6, Sophia Antipolis, France, Sept. 2009.

- Syed Suhaib, Bijoy A. Jose, Deepak A. Mathaikutty, and Sandeep K. Shukla, "Formal Transformation of a KPN specification into a GALS implementation," *Proc. of Forum on Specification and Design Languages (FDL'08)*, pp. 84-89, Germany, Sept. 2008.

- Bijoy A. Jose, Sandeep K. Shukla, Hiren D. Patel, and Jean-Pierre Talpin, "On the Deterministic Multi-threaded Software Synthesis from Polychronous Specifications," *Proc. of the 6th ACM/IEEE International Conference on Formal Models and Methods in Co-Design (MEMOCODE'08)*, pp. 129-138, Anaheim, CA, June 2008.

- Bijoy Jose and Damu Radhakrishnan, "Fast redundant binary partial product generators for Booth multiplication"," *Proc. of 50th IEEE Midwest Symposium on Circuits and Systems (MWSCAS'07)*, pp. 297-300, Montreal, Canada, Aug. 2007.
  [Best Paper Award finalist]

- Bijoy Jose and Damu Radhakrishnan, "Delay Optimized Redundant Binary Adders," *Proc. of 13th IEEE International Conference on Electronics, Circuits and Systems (ICECS),* pp.514 - 517, Nice, France, Dec. 2006.

INDUSTRY PAPERS/POSTERS/WHITE PAPERS

- Bijoy A. Jose, Sushma Thimmappa, Srinivasa Karlapalem, Johnnie Birch, and Kumar Shiv, "A playbook for Analysis, Prototyping and Estimation of optimizations targeting Android Dalvik Virtual Machine", Intel Software Professionals Conference, Santa Clara, USA, 2013. [Best Paper Award]

- Bijoy A. Jose and Abhishek Agrawal, "Energy Efficiency of Virtual Machines," White paper at Intel Developer zone, 2011.

- Bijoy A. Jose, "Formal model driven software synthesis for embedded systems," Ph.D. Dissertation Forum poster at IEEE Design, Automation and Test in Europe (DATE), Grenoble, France, 2011.