DEPARTMENT OF ELECTRONICS
Cochin University of science and Technology

Course Schedule

Course: M.Tech. (Electronics & Communication Engineering)	**Name of Faculty: Dr. Tripti S Warrier**
Topic: 20-437-0111 FPGA Based System Design	**Semester: FIRST**
Lecture Hall: 118	**Timings:** as per CBCS, Slot E

Week and date	*Lecture topics*	*Assignments*	*Remarks*
Week 1 (23rd Nov 20)	• Boolean Algebra and Algebraic Simplification • Combinational Logic - Karnaugh Maps		
Week 2 (30th Nov 20)	• Designing Using NAND and NOR gates • Sequential Circuits – Flip flops, Mealy & Moore Circuits	***Assignment 1***	
Week 3 (7th Dec 20)	• State Reduction • Verilog description of combinational circuits		
Christmas Vacation			
Week 4 (29th Dec 20)	• Behavioral and structural Verilog • Constants, Arrays and • Loops in Verilog	***Assignment 1 submission***	
Week 5 (4th Jan 21)	• Compilation, simulations and synthesis		
Week 6 (11th Jan 21)	• Verification and testbenches		
Week 7 (18th Jan 21)	• Top down Approach to Design		
Week 8 (25th Jan 21)	• Design Examples- BCD Adder, Traffic light Controller	***Assignment 2***	
Week 9 (1st Feb 21)	• Design Examples- Binary Multiplier, Binary Divider		
First Internals			
Week 10 (15th Feb 21)	• Overview of Programmable Devices – CPLD's, FPGA		
Week 11 (22nd Feb 21)	• Implementing functions using FPGAs • Architectures of Commercial FPGAs		
Week 12 (1st Mar 21)	• Cost of programmability • Maximum gates vs usable gates	***Assignment 2 submission***	
Week 13 (8th Mar 21)	• FPGA Design Flow		
Week 14 (15th Mar 21)	• Embedded cores in FPGAs		

Week 15 (22nd Mar 21)	• Case Study System Design using Microblaze softcore processor and Xilinx EDK,		
Second Internals			
Week 16 (29th Mar 21)	• Case Study System Design using built-in ARM Cortex processor and an IP block in PL.		
Week 17 (6th Apr 21)	**Publication of Sessional**		