DEPARTMENT OF ELECTRONICS
Cochin University of science and Technology

Lab Schedule

Course: M.Tech. (Electronics & Communication Engineering)	**Name of Faculty: Dr. Nalesh S**
Topic: 20-437-0106 VLSI Technology Lab	**Semester: FIRST**
Lecture Hall:	**Timings:** as per CBCS

Set of experiments

Experiment 1:Verilog Structural and Dataflow Modeling, Behavioral Modeling
Experiment 2: Modeling Combinational Circuits: Mutiplexers, Encoders, Decoders, Memories
Experiment 3: Tasks, Functions & Testbench
Experiment 4: Modeling Latches and Flip-flops, Registers and Counters
Experiment 5: Familiarization with Cadence Xcelium simulations
Experiment 6: ASIC synthesis using Cadence Genus
Experiment 7: Placement and Routing using Cadence Innovus.
Experiment 8: Familiarization with Cadence Virtuoso schematic editor and Spectre Simulator
Experiment 9: DC and Transient Analysis of a Static CMOS inverter
Experiment 10: DC and Transient Analysis of a complementary CMOS Logic Gates
Experiment 11: Layout using Cadence Virtuoso Layout Editor
Projects: Layout and Characteristics for a combinational logic circuit, RTL, Synthesis and Place and Route for a digital function.