DEPARTMENT OF ELECTRONICS
Cochin University of science and Technology

Course Schedule

Course: M.Tech. (Electronics & Communication Engineering)	**Name of Faculty: Dr.Nalesh S**
Topic: 20-437-0105 VLSI Technology & Design	**Semester: FIRST**
Lecture Hall:	**Timings:** as per CBCS

Week and date	*Lecture topics*	*Assignments*	*Remarks*
Week 1 (23rd Nov 20)	**Module 1: Introduction to CMOS VLSI** MOS transistor Ideal I-V characteristics, NMOS Inverter Circuits and Analysis, Complementary MOS Logic - Inverter, Combinational Logic, NAND/NOR gates, CMOS Fabrication Process -FEOL and BEOL processes		
Week 2 (30th Nov 20)	**Module 2: Combinational Circuit Design** MOSFET capacitances and resistances, Static CMOS Inverter, Static Analysis, Noise Margin	**Class Test-1 Research Topic Selection for Presentation**	
Week 3 (7th Dec 20)	Static CMOS inverter transient response, MOSFET resistance and capacitance, Switching model, Intrinsic Delay, Delay and Sizing	**Class Test-2**	
APSYM 2020			
Week 4 (17th to 22nd Dec 20)	Chain of inverters, Sizing chain of inverters for optimum delay, Power dissipation in static CMOS inverters		
XMAS Vacations			
Week 5 (29th Dec 20)	Complementary CMOS design -Pull up and Pull Down Networks, Static behavior, VTC Dynamic behavior, Delay dependence on Fanin and Fanout, Sizing of Complementary CMOS gates	**Class Test-3**	
Week 6 (4th Jan 21)	Logical Effort, Electrical Effort, Stage Effort, Intrinsic Delay, Sizing an chain of gates. Delay of chain of gates, Critical Path	**Class Test-4**	
Week 7 (11th Jan 21)	Ratioed Logic, Pass-Transistor Logic, Transmission gates, Dynamic Logic, Static Latches and Registers, Dynamic Latches and Registers	**Class Test-5**	
Week 8 (18th Jan 21)	**Module 3: Sequential Circuit Design** Timing Metrics- Setup Time, Hold Time, Propagation Delay, Contamination delay, skew and jitter, Setup and Hold violations	**Research Topic 1st Presentation**	
Week 9 (25th Jan 21)	Classification of Memory Elements, Static Latches and Registers, Dynamic Latches and Registers, Pipelining, Memory Cells	**Class Test-6**	
First Internal Exam			

Week 10 (1st to 12th Feb 21)	**Module 5: CMOS Scaling and Sub-Micron Trends:** Propagation Delays, Logic and Interconnect delays,		
Week 11 (15th Feb 21)	**Module 4: VLSI Design Flow** Custom, Semicustom and Structured-Array Design Approaches, Cell Based Design Methodology, Semicustom Design Flow - Design Capture, Register Transfer Logic, Functional Simulation,	**Class Test-7**	
Week 12 (22nd Feb 21)	High Level Synthesis, Logic Synthesis, Timing Simulation, Static Timing Analysis, Power Analysis, Planning, Partitioning, Placement and Routing, Extraction, Packaging, IC testing		
Week 13 (1st Mar 21)	**Module 1: Introduction to CMOS VLSI** Introduction, Semiconductors, Band Diagrams, Fermi Level, Intrinsic Semiconductor, Doping, P and N type	**Class Test-8**	
Week 14 (8th Mar 21)	Current Transport Mechanisms, PN Junctions, Terminology, Quantitative Analysis, Static Behavior, PN Junction Capacitance,	**Class Test-9**	
Week 15 (15th Mar 21)	MOS Capacitor, Operating regions, Quantitative Analysis, CV characteristics, MOS transistor Ideal I-V characteristics, MOSFET Non Ideal Effects and characteristics	**Class Test-10**	
Second Internal Exam			
Week 16 (22nd Mar to 2nd Apr 21)	**Module 5: CMOS Scaling and Sub-Micron Trends:** Scaling Factors for Device Parameters, Constant field scaling and constant voltage scaling, Challenges going to sub-100 nm MOSFETs		
Week 17 (6th Apr 21)	Multiple gate MOSFETs, FinFETs, Carbon nanotube FET, SpinFET, Nanowire FETs	**Research Topic Final Presentation**	
Week 18 (12th Apr 21)	**Publication of Sessional**		