



<b>Course: M.Tech. (Electronics &amp; Communication Engineering)</b>	<b>Name of Faculty: Dr. Bijoy Antony Jose</b>
<b>Topic: 20-437-0101 Embedded Architecture and Interfacing</b>	<b>Semester: FIRST</b>
<b>Lecture Hall: 118</b>	<b>Timings: as per CBCS - A</b>

<i>Week and date</i>	<i>Lecture topics</i>	<i>Assignments</i>	<i>Remarks</i>
Week 1 (23 Nov 20)	<u><b>Module 1</b></u> <ul style="list-style-type: none"> <li>Review of Processors and Embedded Systems, PIC.</li> <li>Performance and power</li> </ul>		
Week 2 (30 <sup>th</sup> Nov 20)	<ul style="list-style-type: none"> <li>Moore's law, Amdahl's law</li> <li>Review of architectures in academia and industry</li> </ul>		
Week 3 (7 <sup>th</sup> Dec 20)	<ul style="list-style-type: none"> <li>RISC/CISC, Flynn's Classification, Endian-ness</li> <li>Superscalarity, Pipelining</li> </ul>	<b>Assignment-1</b> <ul style="list-style-type: none"> <li>➤ Addressing modes &amp; ISA of x86</li> <li>➤ Problems in parallel processor performance</li> </ul>	
Week 4 (21 <sup>st</sup> Dec 20)	<ul style="list-style-type: none"> <li>Throughput, Latency</li> </ul> <u><b>Module 2</b></u> <ul style="list-style-type: none"> <li>Pentium architecture</li> <li>Pipeline Hazards and conflicts</li> </ul>		
Week 5 (4 <sup>th</sup> Jan 21)	<ul style="list-style-type: none"> <li>Performance optimizations in x86</li> <li>Memory organization</li> <li>Caches, multi-level cache</li> </ul>		
Week 6 (11 <sup>th</sup> Jan 21)	<ul style="list-style-type: none"> <li>Cache placement policies</li> <li>Cache performance</li> <li>Address Translation</li> <li>Paging and virtual memory</li> </ul>	<b>Assignment-1 submission</b>	
Week 7 (18 <sup>th</sup> Jan 21)	<u><b>Module 3</b></u> <ul style="list-style-type: none"> <li>ARM architecture basics</li> <li>Cortex M3 architecture</li> </ul>		
Week 8 (25 <sup>th</sup> Jan 21)	<ul style="list-style-type: none"> <li>Programming mode, registers, NVIC</li> <li>Power management</li> </ul>		
4 <sup>th</sup> Feb 21	First Internals		
Week 9 (15 <sup>th</sup> Feb 21)	<ul style="list-style-type: none"> <li>Multithreaded programming, Graphics processors</li> <li>pThreads, Thread building blocks, GP-GPU</li> </ul>	<b>Assignment-2</b> <ul style="list-style-type: none"> <li>➤ ARM ISA programs</li> <li>➤ Programming Arm and x86 boards</li> </ul>	
Week 10 (22 <sup>nd</sup> Feb 21)	<ul style="list-style-type: none"> <li>Hybrid architectures, GPU</li> <li>NVIDIA CUDA architecture</li> </ul>		

Week 11 (1 <sup>st</sup> Mar 21 )	<b><u>Module 4</u></b> <ul style="list-style-type: none"> <li>• Review of PIC processor ISA</li> <li>• Compare, Capture, PWM</li> <li>• Interrupt handling</li> </ul>		
Week 12 (8 <sup>th</sup> Mar 21)	<ul style="list-style-type: none"> <li>• Timing and interrupts in PIC</li> <li>• Cyber Physical Systems</li> <li>• Internet of Things</li> <li>• Client Server model and cloud computing</li> </ul>		
Week 13 (15 <sup>th</sup> Mar 21)	<ul style="list-style-type: none"> <li>• Edge computing</li> <li>• Arduino, Galileo, Raspberry PI</li> </ul> <b><u>Module 5</u></b> <ul style="list-style-type: none"> <li>• Sensors and transducers</li> <li>• Bluetooth, Zigbee</li> </ul>	<i>Assignment-2 submission</i>	
Week 14 (22 <sup>nd</sup> Mar 21)	<ul style="list-style-type: none"> <li>• Interfacing I2C, SPI, USB</li> <li>• ADC types</li> </ul>		
25 <sup>th</sup> March 21	Second Internals		
Week 15 (5 <sup>th</sup> Apr 21)	<ul style="list-style-type: none"> <li>• Interfacing RTC, PWM, LCD, Stepper motors</li> </ul>		
10 <sup>th</sup> April 21	<i>End of Classes</i>		