



<b>Course: M.Tech. (Electronics &amp; Communication Engineering)</b>	<b>Name of Faculty: Dr.Nalesh S</b>
<b>Topic: 18-437-0108 VLSI Laboratory</b>	<b>Semester: FIRST</b>
<b>Lecture Hall: 213</b>	<b>Timings: as per CBCS</b>

<i>Week and date</i>	<i>Lecture topics</i>	<i>Assignments</i>	<i>Remarks</i>
Week 1 (8 <sup>th</sup> July 19)	<b>Experiment 1:</b> Familiarization with FPGA and Vivado Software Creating new project, add design files and testbench, synthesize and generate bitstream, program the FPGA		
Week 2 (15 <sup>th</sup> July 19)	<b>Experiment 2:</b> Basic Verilog Modeling Concepts  Combinatorial circuits using gate-level, dataflow, and behavioral modelling , Download bitstreams into the board and verify functionality		
Week 3 (22 <sup>nd</sup> July 19)	<b>Experiment 3:</b> Numbering Systems Learn various number representations and arithmetic operations		
Week 4 (29 <sup>th</sup> July 19)	<b>Experiment 4:</b> Multi Output Circuits, Encoders, Decoders Memories  Design multi-output decoder circuits, encoders, ROM		
Week 5 (5 <sup>th</sup> Aug 19)	<b>Experiment 5:</b> Tasks, Functions & Testbench  Develop tasks & functions for modeling a combinatorial circuit  Develop a testbench to test and validate a design under test		
Week 6 (12 <sup>th</sup> Aug 19)	<b>First Internals</b>		
Week 7 (19 <sup>th</sup> Aug 19)	<b>Experiment 6:</b> Modeling Latches and Flip-flops Model various FLIP flops and Latches		
Week 8 (26 <sup>th</sup> Aug 19)	<b>Experiment 7:</b> Modeling Registers and		

	Counters Model various Registers and Counters		
Week 9 (2 <sup>nd</sup> Sep 19)	<b>Experiment 8:</b> Behavioral Modeling and Timing Constraints  Use various language constructs using behavioral modelling. Learn about timing and timing constraints		
<b>Onam Vacation</b>			
Week 10 (17 <sup>th</sup> Sep 19 )	<b>Experiment 9:</b> Finite State Machines Verilog modeling of FSMs		
Week 11 (23 <sup>rd</sup> Sep 19)	<b>Experiment 10:</b> Introduction to DCH and Microwind		
Week 12 (30 <sup>th</sup> Sep 19)	<b>Experiment 11:</b> Study static and dynamic behavior of Static CMOS Inverter		
Week 13 (7 <sup>th</sup> Oct 19)	<b>Experiment 12:</b> Complementary CMOS circuits		
Week 14 (14 <sup>th</sup> Oct 19)	<b>Experiment 13:</b> Layout of CMOS gates using MicroWind		
Week 15 (21 <sup>st</sup> Oct 19)	<b>Experiment 14:</b> Multiplication with Repeated addition, Modeling, Simulation and verification.		
Week 16 (28 <sup>th</sup> Oct 19)	<b>Second Internals</b>		
Week 17 (6 <sup>th</sup> Nov 19)	<b>Publication of Sessional</b>		