DEPARTMENT OF ELECTRONICS
Cochin University of science and Technology

Course Schedule

Course: M.Tech. (Electronics & Communication Engineering)	**Name of Faculty: Dr.Nalesh S**
Topic: 18-437-0107 VLSI Technology & Design	**Semester: FIRST**
Lecture Hall: 118	**Timings:** as per CBCS

Week and date	*Lecture topics*	*Assignments*	*Remarks*
Week 1 (8th July 19)	**Module 1: Introduction to CMOS VLSI** Introduction, Semiconductors, Band Diagrams, Fermi Level, Intrinsic Semiconductor, Doping, P and N type, Current Transport Mechanisms PN Junctions, Terminology, Quantitative Analysis, Static Behavior		
Week 2 (15th July 19)	PN Junction Capacitance, MOS Capacitor, Operating regions, Quantitative Analysis	**Class Test-1 Research Topic for Presentation**	
Week 3 (22nd July 19)	MOS Capacitor CV characteristics, MOS transistor Ideal I-V characteristics, MOSFET Non Ideal Effects, NMOS Inverters	**Class Test-2**	
Week 4 (29th July 19)	MOSFET capacitances and resistances, Complementary MOS Logic - Inverter, Combinational Logic, NAND/NOR gates **Module 2: Combinational Circuit Design** Static CMOS Inverter, Static Behavior, Static CMOS Inverter, Dynamic Behavior, Transient Response	**Class Test-3**	
Week 5 (5th Aug 19)	Static CMOS Inverter, resistance and capcitance model, Sizing of Inverters, Sizing chain of inverters for optimum delay, Power dissipation in static CMOS inverters	**Class Test-4**	
Week 6 (12th Aug 19)	**First Internals**		
Week 7 (19th Aug 19)	Complementary CMOS design -Pull up and Pull Down Networks, Static behavior, VTC Dynamic behavior, Delay dependence on Fanin and Fanout, Sizing of Complementary CMOS gates	**Class Test-5**	
Week 8 (26th Aug 19)	Logical Effort, Sizing an chain of gates,	**Presentation-1**	
Week 9 (2nd Sep 19)	Ratioed Logic, Pass-Transistor Logic, Transmission gates, Dynamic Logic, Static Latches and Registers, Dynamic Latches and Registers	**Class Test-6**	
Onam Vacation			

Week 10 (17th Sep 19)	Pipelining, Time borrowing, Timing Metrics, Memory Cells		
Week 11 (23rd Sep 19)	**Module 4: CMOS Fabrication and Layout** Fabrication Process -Silicon wafer preparation, FEOL processing, Diffusion of impurities, ion implantation, annealing, oxidation, lithography	**Class Test-7**	
Week 12 (30th Sep 19)	Chemical Vapour Deposition, epitaxial growth, BEOL process- metallization, patterning, wire bonding, packaging. MOS Layers, Layout Design Rules, Gate Layout		
Week 13 (7th Oct 19)	**Module 5: CMOS Scaling and Sub-Micron Trends:** Propagation Delays, Logic and Interconnect delays, Scaling Factors for Device Parameters, Constant field scaling and constant voltage scaling	**Presentation-2**	
Week 14 (14th Oct 19)	Challenges going to sub-100 nm MOSFETs Multiple gate MOSFETs, FinFETs, Silicon-on-insulator	**Class Test-8**	
Week 15 (21st Oct 19)	**Module 3: VLSI Design Flow** Custom, Semicustom and Structured-Array Design Approaches, Semicustom Design Flow Design Capture, Register Transfer Logic, Functional, Simulation, High Level Synthesis, Logic Synthesis, Timing Simulation, Static Timing Analysis, Power Analysis, Planning, Partitioning, Placement and Routing, Extraction, Packaging, IC testing		
Week 16 (28th Oct 19)	**Second Internals**		
Week 17 (6th Nov 19)	**Publication of Sessional**		