DEPARTMENT OF ELECTRONICS
Cochin University of science and Technology

Course Schedule

Course: M.Sc. (Electronic Science)	**Name of Faculty: Dr. Nalesh S**
Topic: 18-305-0302 VLSI Design	**Semester: THIRD**
Lecture Hall: 112	**Timings:** as per CBCS

Week and date	*Lecture topics*	*Assignments*	*Remarks*
Week 1 (1st July 19)	**Module 1: MOSFET Device Physics:** Semiconductor Band Diagrams, Fermi Level, Intrinsic Semiconductor ,Doping, P and N type, Current Transport Mechanisms, PN Junctions , Static and Dynamic Behavior, Junction Capacitance		
Week 2 (8thJuly 19)	MOS Transistor, Cross Section MOS capacitor, Operating modes, C-V Characteristics , Ideal I-V Characteristics		
Week 3 (15th July 19)	MOS Transistor C-V Characteristics, Ideal I-V Characteristics, Non-Ideal I-V Effects		
Week 4 (22nd July 19)	**Module 2: CMOS Technology:** NMOS Inverters, Complementary MOS Logic – Inverter, Cross Section, Complementary MOS Logic – Inverter, Cross Section, Pull Up, Pull Down Network, Complex gates, Combinational Logic ,NAND/NOR gates, Complex Gates	**Assignment-1**	
Week 5 (29th July 19)	Fabrication Process , Introduction, Crystal Growth, Lithography, Diffusion, Ion Implantation, CVD, metallization, Latch-up in CMOS, Introduction to VLSI Design Flow		
Week 6 (5th Aug 19)	**Module 3: Combinational Circuits:** Static CMOS Circuits, Static and Dynamic Circuits, Advantages, Disadvantages, Static CMOS Inverter, Static Behavior, Static CMOS Inverter, Dynamic Behavior		
Week 7 (12th Aug 19)	**Seminar**		
Week 8 (19th Aug 19)	CMOS delay model, Sizing a chain of inverters, Logical Effort, Sizing a chain of gates		
Week 9 (26th Aug 19)	Ratioed Logic, Pass-Transistor Logic, Transmission gates, Dynamic CMOS Circuits	**Assignment-1 Submission**	
Week 10 (2nd Sep 19)	**Module 4: Sequential Circuits:** Classification of Memory Elements, Static Latches and Registers. Dynamic Latches and Registers		
Onam Vacation			
Week 11 (16th Sep 19)	**First Internals**		
Week 12 (23rd Sep 19)	Timing Metrics, Propagation Delay, Setup time, Hold Time, Pipelining	**Assignment-2**	
Week 13 (30th Sep 19)	Pipelining		

Week 14 (7th Oct 19)	**MOS Circuit Design:** Layouts, – layout layers, layout of inverter layouts of 2-input NAND gate and 2-input NOR gate Design rules and layout – layouts of 2-input NAND gate and 2-input NOR gate		
Week 15 (14th Oct 19)	**Second Internals**		
Week 16 (21st Oct 19)	**<u>Module 5:</u> Delay, Power Dissipation and Scaling in MOS:** Concept of sheet resistance and capacitances Interconnect delay and modeling using Elmore delay	**Assignment-2 Submission**	
Week 17 (28th Oct 19)	Power dissipation – Static and dynamic power dissipation, Scaling – scaling models and factors, constant field and voltage scaling Limitations of scaling.		
Week 18 (6th Nov 19)	**Publication of Sessional**		