DEPARTMENT OF ELECTRONICS
Cochin University of science and Technology

Course Schedule

Course: M.Sc. (Electronic Science)	**Name of Faculty: Mithun Haridas T.P.**
Topic: 16-305-0105 DIGITAL SYSTEM DESIGN	**Semester: FIRST**
Lecture Hall: MSc 1st **(Electronic Science)**	**Timings:** as per CBCS

Week and date	*Lecture topics*	*Assignments*	*Remarks*
Week 1 (10th July 19)	• Module 1: Review of Digital Systems • Truth Tables, Laws and Theorems of Boolean algebra • Min-term and Max-term Expansions, K-maps • Quine-McCluskey Method		
Week 2 (15thJuly 19)	• Combinational logic circuits • code converters, adder, subtractor, magnitude comparator, • decoder, encoder, multiplexer		
Week 3 (22nd July 19)	• Module 4: Introduction to HDL • VHDL: Terms, Object types, Data types, Operators, • Design units, Sub programs and Packages, Libraries • Concurrent Statements, Sequential Statements	***Assignment-1*** • **Modeling of Combinational logic circuit using VHDL**	
Week 4 (29thJuly 19)	• Behavioral, Data flow, Structural Modeling, • Test Bench • Compilation and Simulation of VHDL Code		
Week 5 (5th Aug 19)	• Module 2: Digital Logic Design • Latches, Flip-Flops, Sequential Circuits		
Week 6 (12thAug 19)	• Analysis of clocked sequential circuits • Mealy and Moore Models • state-transition table, state diagram	***Assignment-1 submission***	
Week 7 (19thAug 19)	• state reduction and assignment, design procedures		

	• Finite State Machine design, • Registers and Counters, Hazards		
Week 8 (26th Aug 19)	First Internals		
Week 9 (2nd Sep 19)	• Module 5: System Design using VHDL • Realization of combinational and sequential circuits using HDL	***Assignment-2*** ➢ Modeling Sequential Circuits using VHDL	
Week 10 (16th Sep 19)	• Modeling Flip-Flops, Registers, Counters, • Modeling of Mealy and Moore finite state machines		
Onam Vacation			
Week 11 (23rd Sep 19)	• Module 3: Electronic Design Automation Tools • Introduction to EDA tools • Design flow and levels of abstraction	***Assignment-2 submission***	
Week 12 (30thSep 19)	• Design automation at logic level • Design Methodology		
Week 13 (14th Oct 19)	Second Internals		
Week 14 (21st Oct 19)	• Two level and Multi level logic synthesis • Transformations on Boolean networks,		
Week 15 (28thOct 19)	*Revision: System Design for practical problems (Discussions)		
Week 16 (4th Nov 19)	*Revision: System Design for practical problems (Discussions)		
Week 17 (6th Nov 19)	*Publication of Sessional*		
Week 18 (7th Nov 19)	**REVISION**		