Sponsorship Certificate

Workshop on ASIC Front-End Design Flow

2019, April 5 - 6

Department of Electronics
Cochin University of Science & Technology
Kochi-22, Kerala

Certified that Dr./Mr./Ms..... is working as ..... in our Institution /Organization and is hereby sponsored to attend Workshop on ASIC Front-End Design Flow to be held at Department of Electronics, CUSAT, Kochi-22, Kerala, from April 05-06, 2019. He/She will be permitted to attend the entire programme, if selected.

Email ID:

Mobile No.

Signature and seal of
Sanctioning authority

Place:

Date:

Contact Details of Co-ordinator

Dr. Tripti S Warrier
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Cochin University of Science & Technology
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Kerala.
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2-Day Workshop on

ASIC Front-End Design Flow

2019, April 05 - 06

Organized by

Department of Electronics
Cochin University of Science & Technology
Kochi-22, Kerala

In association with

CoreEL Technologies (I) Pvt Ltd
and
IEEE Computer Society Kerala Chapter

Registration Details

- Rs. 500 for Students
- Rs. 1000 for Faculty

Confirm your participation by applying through the link provided on or before 3/04/2019.
Registration link :
https://goo.gl/forms/qRPfUQUEb4fGBbJu1

N.B. Participants may be requested to bring their own laptops to attend the workshop

Resource Person

Prakash G, Lead Application Engineer,
CoreEL Technologies (I) Pvt Ltd

Programme Schedule

Day 1

- Basic of Verilog and SystemVerilog
- Brief Description on latest Simualtor and synthesis tools
- Advance SystemVerilog Constructs
- Simulation of SystemVerilog Code for basic design using Questasim Simulator
- Simulator tool flow and Improved designs flow model
- Introduction of different types of Testbench Architectures
- Code Coverage and Function coverage reports
- Bus functional Models and Verification IP methods

Day 2

- Synthesis flow using Leonardo Spectrum
- DFT Tessent tool
- Introduction to Design for Testability (DFT)
- Post Synthesis Verification techniques.
- DFT Scan & Automatic test pattern generation (ATPG)
- Tessent DFTAdvisor tool(for scan chain Insertion)